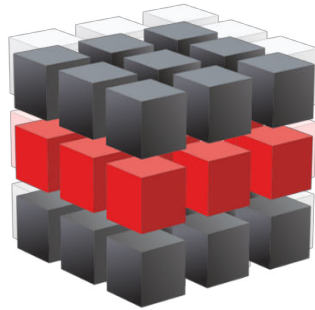




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www.micansinfotech.com | micansinfotech@gmail.com
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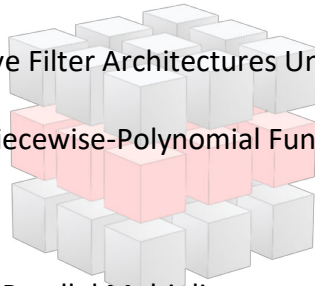
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VERY LARGE SCALE INTEGRATION 2020-2021

New Titles

1. Multistage Linear Feedback Shift Register Counters With Reduced Decoding Logic in 130-nm CMOS for Large-Scale Array Applications
2. Hybrid Logical Effort for Hybrid Logic Style Full Adders in Multistage Structures
3. A 1.2-V 2.41-GHz Three-Stage CMOS OTA With Efficient Frequency Compensation Technique
4. Robust Proportionate Adaptive Filter Architectures Under Impulsive Noise
5. Dual-Channel Multiplier for Piecewise-Polynomial Function Evaluation for Low-Power 3D Graphics
6. A Two-Speed, Radix-4, Serial-Parallel Multiplier
7. Designing Efficient Circuits Based on Runtime-Reconfigurable Field-Effect Transistors
8. Three-Dimensional Monolithic FinFET-Based 8T SRAM Cell Design for Enhanced Read Time and Low Leakage
9. Efficiently Mapping VLSI Circuits With Simple Cells
10. A Carry Lookahead Adder Based on Hybrid CMOS-Memristor Logic Circuit
11. Optimization Design on Active Guard Ring to Improve Latch-Up Immunity of CMOS Integrated Circuits
12. A 7T-SRAM With Data-Write Technique by Capacitive Coupling
13. Adaptively Biased Output Cap-Less NMOS LDO With 19 ns Settling Time
14. A 60GHz CMOS Power Amplifier with Parametric Matching Networks-(ADS Software)
15. A CMOS PUF Circuit Primitive Based on a Two-Dimensional Nonlinear Dynamical System -(ADS Software)





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16. A Digital-to-Time Converter with Coupled Phase- Rotating LC Oscillators in 90-nm

CMOS Technology-(ADS Software)

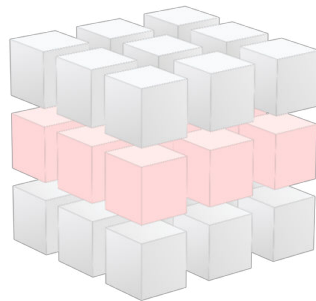
17. A Low Noise Fault Tolerant Radiation Hardened 2.56 Gbps Clock-Data Recovery Circuit

with High Speed Feed Forward Correction in 65 nm CMOS. -(ADS Software)

18. CMOS implementation of wide frequency bandwidth Resonator's Q-factor

measurement circuit.

19. Design of Low Leakage SRAM Bitcell



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