Array-Based Approximate Arithmetic Computing A General Model and Applications to Multiplier and Squarer Design

ABSTRACT

We proposea general mode lfor array-basedapprox-imate arithmetic computing (AAAC) to guide the minimization of processing error. As part of this model, the Error Compensation Unit (ECU) is identified as a key building block for a wide range of AAAC circuits. We develop theoretical analysis geared towards addressing two critical design problems of the ECU,namely, determination of optimal error compensation values and identification of the optimal error compensation scheme. We demonstrate how this general AAAC model can be

leveraged to derive practical design insights that lead to optimal tradeoffs between accuracy, Energy dissipation and area over head. To further minimize energy consumption, delay and area of AAAC circuits. We perform ECU Designs implification by introducing logic don't cares.By applying this model and using a commercial 90 nm CMOS standard cell library, we propose an approximate 16 16 fixed width Booth multiplier that consumes 44.85% and 28.33%less energy and area compared with theoretically the most accurate fixed-width Booth multiplier. Furthermore, it reduces average error, max error and meansquarederrorby11.11%,28.11%,and25.00%,respectively, when compared with the most accurate reported approximate Booth multiplier and outperforms the same design significantly by 19.10% for the energy-delay-mean squared error product.Using the same approach, significant energy consumption, area and error reduction is achieved for a squarer unit. To further Reduce error and cost by utilizing extra signatures and don'tcares, we demonstrate a 16-bit fixed-width squarer that improves the energy-delay-max error product by 15.81%.

EXISTING SYSTEM

An approximate AND-array multi-pliers, which utilize AND gates for partial product generation and approximate Booth multipliers, which use the modified Booth algorithm to reduce the number of partial products.Statistical linear regression analysis, estimation threshold calculation, and self compensation approach have been utilized to compensate the truncation error.

PROPOSED SYSTEM

To shed light on the design of ECU, which is the key of AAAC design, we develop four theorems to address two critical design problems of the ECU design, namely, determination of optimal error compensation values and identification of the optimal error compensation scheme.To further reduce energy consumption and area, we introduce don't cares for ECU logic simplification.

SYSTEM REQUIERMENTS

Microwind/tanner

REFERENCES

[1] M. J. Schulte and E. E. Swartzlander, “Truncated multiplication with correction constant,”Proc. Workshop VLSI Signal Processing VI, pp. 388–396, 1993.

[2]E.J.KingandE.E.Swartzlander,“Data dependent truncation scheme for parallel multipliers,”Conf. Rec. 31st Asilomar Conf. Signals, Syst. Comput., 1997.