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### VLSI Title lists

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- 3) Automatic ReRAM SPICE Model Generation From Empirical Data for Fast ReRAM-Circuit Coevaluation- February 2017
- 4) Analytical Models of High-Speed RLC Interconnect Delay for Complex and Real Poles-February 2017
- 5) Double-Node-Upset-Resilient Latch Design for Nanoscale CMOS Technology- February 2017
- 6) All-Digital Calibration of Timing Mismatch Error in Time-Interleaved Analog-to-Digital Converters-May 2017
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