Zero-Power Feed-Forward Spur Cancelation for Supply Regulated CMOS Ring PLLs

ABSTRACT

- The proposed technique achieves a simulated spur cancelation of about 22 dB at the first spur harmonic.
- Spur cancelation is also robust against large process, voltage, and temperature variations in the gain and bandwidth of the FF path.
- A 1-GHz integer-N PLL prototype in a 65-nm CMOS process has a measured cancelation of 19.5 and 13 dB at the first and the second spur harmonic, respectively, with 320μW of total power consumption.

EXISTING SYSTEM

- A new reference-spur cancelation technique is presented for supply-regulated ring-oscillator-based integer-N phase-locked loops.
- A passive RC filter is used to implement a feed-forward spur-coupling path to perform spur cancelation at the PLL control signal.
- The spectral purity of a PLL output is quantified as the relative strength of the phase noise and the spurious tones compared to the LO signal.

PROPOSED SYSTEM

- This paper presents a novel FF spur cancelation technique for supply-regulated ring PLLs.
- Up to the third spur harmonics are canceled significantly by introducing a passive high-pass filter-based FF spur-coupling pat.
- The proposed technique has low complexity and zero power consumption, which makes it suitable for the design of low-power PLLs for low-cost applications.

HARDWARE REQUIREMENTS

- Processor - intel core i3
- RAM - 2GB
- Hard Disk - 20 GB

SOFTWARE REQUIREMENTS

- Tool - MICRO WIND
- Operating system - Windows 7,8

REFERENCE

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