Bandwidth Enhancement to Continuous-Time Input Pipeline ADCs

ABSTRACT

This paper presents design analysis and insights for a new continuous-time input pipeline (CTIP) analog-to-digital converter (ADC) architecture that has enhanced bandwidth. An all-pass filter-based analog delay in the signal path allows bandwidth extension to Nyquist signal bandwidths. A resetting integrator gain stage provides a signal path delay helping to increase the bandwidth while reducing the power cost. The noise filtering property of the resetting integrator gain stage preserves the medium resistive input benefit of CTIP ADCs. The resetting integrator allows the architecture to be implemented with a feedforward compensated op-amp using low-voltage CMOS processes. This paper has been verified by simulation results of a CTIP ADC with 1.2-V supply voltage designed in TSMC's 65-nm CMOS technology.

EXISTING SYSTEM

- CT sigma delta (CT) ADCs are a widely adopted CT ADC architecture. CT ADCs scale with process and new architectures are leading to performance improvements and much lower power consumption.
- The major drawback with CT is that they require gigahertz clocks with very low clock jitter, and the power requirement of generating these clocks is too expensive in applications where such a clock is not already present.
- Intersymbol interference (ISI) in the feedback DACs limits the performance of CT ADCs with larger than single-bit feedback DACs. CT ADCs also have a feedback loop with memory so they cannot be used in applications where different input signals are multiplexed to a common ADC.

PROPOSED SYSTEM

- We propose a new CTIP architecture that can achieve signal bandwidths close to the Nyquist frequency.
- An all-pass filter (APF) is demonstrated as an analog delay and redundancy in the frontend compensates for any phase nonlinearity.
- The signal delay benefits of resetting integrator gain stages that allow increased signal bandwidths.
- Also, the noise filtering benefit of resetting integrator gain stages that preserves the medium resistive input benefit of CTIP ADCs. The gain stage topology permits implementation using a feedforward (FF) compensated op-amp which is a low voltage and lower power solution.

SYSTEM REQUIREMENTS

HARDWARE REQUIREMENTS:

- Processor - intel core i3
- RAM - 2GB
- Hard Disk - 20 GB

SOFTWARE REQUIREMENTS:

- Tool - Tanner/Microwind

REFERENCE

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