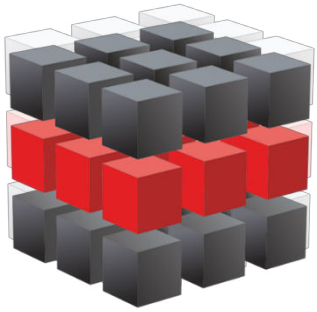
MICANS Infotech
Innovations For Business



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VERY LARGE SCALE INTEGRATION 2018-2019

New Titles

1. High-Throughput Area-Efficient Processor for Cryptography
2. A CMOS Ultra wideband Pulse Generator for 3–5 GHz Applications
3. A Power-Efficient Reconfigurable Output-Capacitor-Less Low-Drop-Out Regulator for Low-Power Analog Sensing Front-End
4. Analysis and Design of the Classical CMOS Schmitt Trigger in Subthreshold Operation
5. 28-nm Latch-Type Sense Amplifier Modification for Coupling Suppression
6. Low-Computing-Load, High-Parallelism Detection method based on Chebyshev Iteration for Massive MIMO Systems with VLSI Architecture
7. Novel Radiation-Hardened-by-Design (RHBD)12T Memory Cell for Aerospace Applications in Nanoscale CMOS Technology
8. VLSI Implementation of a Cost-Efficient Micro Control Unit With an Asymmetric Encryption for Wireless Body Sensor Networks
9. Ultra-Low Power, Highly Reliable, and Nonvolatile Hybrid MTJ/CMOS Based Full-Adder for Future VLSI Design
10. Reliability Enhancement of Low-Power Sequential Circuits Using Reconfigurable Pulsed Latches
11. Area and Energy-Efficient Complementary Dual-Modular Redundancy Dynamic Memory for Space Applications
12. Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers
13. Design of Power and Area Efficient Approximate Multipliers
14. RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing
15. A Compact-Area Low-VDD min 6T SRAM With Improvement in Cell Stability, Read Speed, and Write Margin Using a Dual-Split-Control-Assist Scheme
16. Stable, Reliable and Bit-Interleaving 12T SRAM for Space Applications: A Device Circuit Co-design
17. "Pre-Charged Local Bit-Line Sharing SRAM Architecture for Near-Threshold Operation

18. Language: CMOS Design"
19. 10T SRAM Using Half-VDD Precharge and Row-Wise Dynamically Powered Read Port for Low Switching Power and Ultralow RBL Leakage
20. Content Addressable Memory—Early Predict and Terminate Precharge of Match-Line
21. Modeling and Mitigation of Static Noise Margin Variation in Subthreshold SRAM Cells
22. Designing RF Ring Oscillator using Current-mode Technology
23. A Low-Energy Machine-Learning Classifier Based on Clocked Comparators for Direct Inference on Analog Sensors
24. Single-Event Performance of Sense-Amplifier Based Flip-Flop Design in a 16-nm Bulk FinFET CMOS Process
25. Design of Approximate Radix-4 Booth Multipliers for Error Tolerant Computing
26. Design of Low-Voltage High-Speed CML D-Latches in Nanometer CMOS Technologies
27. Low power-delay-product dynamic CMOS circuit design techniques
28. A Power-Efficient Signal-Specific ADC for Sensor-Interface Applications
29. OTA-Based Logarithmic Circuit for Arbitrary Input Signal and Its Application

VLSI

1) Low-Cost Sorting Network Circuits Using Unary Processing.
2) Algorithm and VLSI Architecture Design of Proportionate-Type LMS Adaptive Filters for Sparse System Identification.
3) Taming Spatiotemporal Chaos in Forced Memristive Arrays.
4) Bandwidth Enhancement to Continuous-Time Input Pipeline ADCs.
5) A DfT Insertion Methodology to Scannable Q-Flop Elements.
6) A Dual-Data Line Read Scheme for High-Speed Low-Energy Resistive Nonvolatile Memories.
7) Single-Chip Design for Intelligent Surveillance System.
8) High-Density SOT-MRAM Based on Shared Bitline Structure.
9) A Changing-Reference Parasitic-Matching Sensing Circuit for 3-D Vertical RRAM.

10) Design and Analysis of Energy-Efficient and Reliable 3-D ReRAM Cross-Point Array System.
11) A Changing-Reference Parasitic-Matching Sensing Circuit for 3-D Vertical RRAM.
12) Stateful Memristor-Based Search Architecture.
13) Robust Design-for-Security Architecture for Enabling Trust in IC Manufacturing and Test.
14) DCMCS: Highly Robust Low-Power Differential Current-Mode Clocking and Synthesis.
15) Viewer-Aware Intelligent Efficient Mobile Video Embedded Memory.
16) Scalable Symbolic Simulation-Based Automatic Correction of Modern Processors.
17) Configurable Logic Operations Using Hybrid CRS-CMOS Cells.
18) Thermal Management of Batteries Using Supercapacitor Hybrid Architecture With Idle Period Insertion Strategy.
19) Three-Dimensional Pipeline ADC Utilizing TSV/ Design Optimization and Memristor Ratioed Logic.
20) Energy- and Area-Efficient Spin–Orbit Torque Nonvolatile Flip-Flop for Power Gating Architecture.
21) Cascade and LC Ladder-Based Filter Realizations Using Synchronous Time-Mode Signal Processing.
22) Multilevel Half-Rate Phase Detector for Clock and Data Recovery Circuits.
23) Zero-Power Feed-Forward Spur Cancelation for Supply-Regulated CMOS Ring PLLs.
24) Systematic Design of an Approximate Adder: The Optimized Lower Part Constant-OR Adder.
25) VOSsim: A Framework for Enabling Fast Voltage Overscaling Simulation for Approximate Computing Circuits.
26) Vector Processing-Aware Advanced Clock-Gating Techniques for Low-Power Fused Multiply-Add.
27) On Synthesizing Memristor-Based Logic Circuits With Minimal Operational Pulses.
28) Secure Double Rate Registers as an RTL Countermeasure Against Power Analysis Attacks.
29) Duty-Cycle-Based Controlled Physical Unclonable Function.
30) Improving Error Correction Codes for Multiple-Cell Upsets in Space Applications.
31) Toward an Energy-Efficient High-Voltage Compliant Visual Intracortical Multichannel Stimulator.

32) Design Considerations for Energy-Efficient and Variation-Tolerant Nonvolatile Logic.

33) Stream Processing Dual-Track CGRA for Object Inference.

34) Toward Energy-Efficient Stochastic Circuits Using Parallel Sobol Sequences.

35) An Electrical Model for Nanometer CMOS Device Stress Effect in Design and Simulation of Analog Reference Circuits

36) CMOS Gates with Second Function

37) CMOS Oscillator having Stable Frequency with Process, Temperature and Voltage Variation

38) Design of Divider Circuit for Electrochemical Impedance Spectroscopy Measurement System

39) A 7-nm Dual Port 8T SRAM with Duplicated Inter-Port Write Data to Mitigate Write Disturbance

40) 2nd Order Sallen Key Switched Capacitor LPF with N-type Transistors

41) A 0.6 mW 1.6 dB Noise Figure Inductorless Shunt Feedback Wideband LNA With Gm Enhancement and Current Reuse in 65 nm CMOS

42) Parasitic Aware Automatic Analog CMOS Circuit Design Environment using ABC Algorithm

43) An Ultra Low Power, 10-bit Two-Step Flash ADC for Signal Processing Applications

44) Area efficient NMOS based positive and negative voltage multiplier

45) CMOS Current-Reversing Circuit

46) A 25- Gb/s 13 mW Clock and Data Recovery Using C^2Mos D-Flip-Flop in 65-nm CMOS