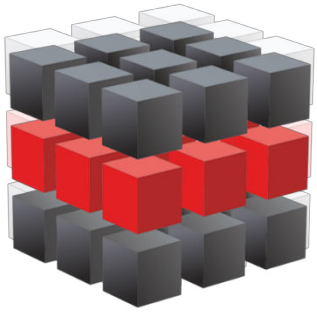
MICANS Infotech
Innovations For Business



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CHENNAI – PONDICHERRY

VERY LARGE SCALE INTEGRATION 2018-2019

1) Low-Cost Sorting Network Circuits Using Unary Processing.
2) Algorithm and VLSI Architecture Design of Proportionate-Type LMS Adaptive Filters for Sparse System Identification.
3) Taming Spatiotemporal Chaos in Forced Memristive Arrays.
4) Bandwidth Enhancement to Continuous-Time Input Pipeline ADCs.
5) A DfT Insertion Methodology to Scannable Q-Flop Elements.
6) A Dual-Data Line Read Scheme for High-Speed Low-Energy Resistive Nonvolatile Memories.
7) Single-Chip Design for Intelligent Surveillance System.
8) High-Density SOT-MRAM Based on Shared Bitline Structure.
9) A Changing-Reference Parasitic-Matching Sensing Circuit for 3-D Vertical RRAM.
10) Design and Analysis of Energy-Efficient and Reliable 3-D ReRAM Cross-Point Array System.
11) A Changing-Reference Parasitic-Matching Sensing Circuit for 3-D Vertical RRAM.
12) Stateful Memristor-Based Search Architecture.
13) Robust Design-for-Security Architecture for Enabling Trust in IC Manufacturing and Test.
14) DCMCS: Highly Robust Low-Power Differential Current-Mode Clocking and Synthesis.
15) Viewer-Aware Intelligent Efficient Mobile Video Embedded Memory.
16) Scalable Symbolic Simulation-Based Automatic Correction of Modern Processors.
17) Configurable Logic Operations Using Hybrid CRS-CMOS Cells.
18) Thermal Management of Batteries Using Supercapacitor Hybrid Architecture With Idle Period Insertion Strategy.
19) Three-Dimensional Pipeline ADC Utilizing TSV/ Design Optimization and Memristor Ratioed Logic.
20) Energy- and Area-Efficient Spin–Orbit Torque Nonvolatile Flip-Flop for Power Gating Architecture.
21) Cascade and LC Ladder-Based Filter Realizations Using Synchronous Time-Mode Signal Processing.
22) Multilevel Half-Rate Phase Detector for Clock and Data Recovery Circuits.
23) Zero-Power Feed-Forward Spur Cancelation for Supply-Regulated CMOS Ring PLLs.

24) Systematic Design of an Approximate Adder: The Optimized Lower Part Constant-OR Adder.
25) VOSsim: A Framework for Enabling Fast Voltage Overscaling Simulation for Approximate Computing Circuits.
26) Vector Processing-Aware Advanced Clock-Gating Techniques for Low-Power Fused Multiply-Add.
27) On Synthesizing Memristor-Based Logic Circuits With Minimal Operational Pulses.
28) Secure Double Rate Registers as an RTL Countermeasure Against Power Analysis Attacks.
29) Duty-Cycle-Based Controlled Physical Unclonable Function.
30) Improving Error Correction Codes for Multiple-Cell Upsets in Space Applications.
31) Toward an Energy-Efficient High-Voltage Compliant Visual Intracortical Multichannel Stimulator.
32) Design Considerations for Energy-Efficient and Variation-Tolerant Nonvolatile Logic.
33) Stream Processing Dual-Track CGRA for Object Inference.
34) Toward Energy-Efficient Stochastic Circuits Using Parallel Sobol Sequences.

35) An Electrical Model for Nanometer CMOS Device Stress Effect in Design and Simulation of Analog Reference Circuits
36) CMOS Gates with Second Function
37) CMOS Oscillator having Stable Frequency with Process, Temperature and Voltage Variation
38) Design of Divider Circuit for Electrochemical Impedance Spectroscopy Measurement System
39) A 7-nm Dual Port 8T SRAM with Duplicated Inter-Port Write Data to Mitigate Write Disturbance
40) 2nd Order Sallen Key Switched Capacitor LPF with N-type Transistors

41) A 0.6 mW 1.6 dB Noise Figure Inductorless Shunt Feedback Wideband LNA With Gm Enhancement and Current Reuse in 65 nm CMOS

42) Parasitic Aware Automatic Analog CMOS Circuit Design Environment using ABC Algorithm

43) An Ultra Low Power, 10-bit Two-Step Flash ADC for Signal Processing Applications

44) Area efficient NMOS based positive and negative voltage multiplier

45) CMOS Current-Reversing Circuit

46) A 25- Gb/s 13 mW Clock and Data Recovery Using C^2Mos D-Flip-Flop in 65-nm CMOS