

- 10+ Years of Excellence in IEEE Project development for universities across INDIA, USA, UK, AUSTRALIA, SWEDEN.
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VLSI Title list

- 1) Excavating the Hidden Parallelism Inside DRAM Architectures With Buffered Comparers- February 2017
- 2) Cross-Layer Optimization for Multilevel Cell STT-RAM Caches-February 2017
- 3) Automatic ReRAM SPICE Model Generation From Empirical Data for Fast ReRAM-Circuit Coevaluation- February 2017
- 4) Analytical Models of High-Speed RLC Interconnect Delay for Complex and Real Poles-February 2017
- 5) Double-Node-Upset-Resilient Latch Design for Nanoscale CMOS Technology- February 2017
- 6) All-Digital Calibration of Timing Mismatch Error in Time-Interleaved Analog-to-Digital Converters-May 2017
- 7) Self-Controlled High-Performance Precharge-Free Content-Addressable Memory-April 2017
- 8) Maximizing Common Idle Time on Multicore Processors With Shared Memory-March 2017
- 9) A 0.1–2-GHz Quadrature Correction Loop for Digital Multiphase Clock Generation Circuits in 130-nm CMOS-MAR 2017
- 10) Tri-modal Scan-Based Test Paradigm-MAR 2017
- 11) High Performance Parallel Decimal Multipliers Using Hybrid BCD Codes-MAY 2017

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- 12) A High-Speed and Power-Efficient Voltage Level Shifter for Dual-Supply Applications-MAR 2017
- 13) High-Density 4T SRAM Bitcell in 14-nm 3-D CoolCube Technology Exploiting Assist Techniques- APRIL 2017
- 14) Leveraging Unused Resources for Energy Optimization of FPGA Interconnect-MAY 2017
- 15) A 50-mA 99.2% Peak Current Efficiency, 250-ns Settling Time Digital Low-Dropout Regulator With Transient Enhanced PI Controller-MARCH 2017
- 16) Design of Temperature-Aware Low-Voltage 8T SRAM in SOI Technology for High-Temperature Operation (25 °C–300 °C)-APRIL 2017
- 17) Self-Controlled High-Performance Precharge-Free Content-Addressable Memory- APRIL 2017.
- 18) A Noise-Power-Area Optimized Biosensing Front End for Wireless Body Sensor Nodes and Medical Implantable Devices-JUNE 2017
- 19) High-Current Drivability Fibonacci Charge Pump With Connect–Point–Shift Enhancement- MARCH 2017
- 20) An On-Chip Monitoring Circuit for Signal-Integrity Analysis of 8-Gb/s Chip-to-Chip Interfaces With Source-Synchronous Clock-january 2017
- 21) Scalable Device Array for Statistical Characterization of BTI-Related Parameters-January 2017

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- 22) Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers- January 2017
- 23) A 32-nm Subthreshold 7T SRAM Bit Cell With Read Assist
- 24) Design of Low-Voltage High-Speed CML D-Latches in Nanometer CMOS Technologies
- 25) Power-Gated 9T SRAM Cell for Low-Energy Operation
- 26) A Variation-Tolerant Near-Threshold Processor with Instruction-Level Error Correction- MARCH 2017
- 27) A CMOS Ultra wideband Pulse Generator for 3–5 GHz Applications-MAY 2017
- 28) Analytical Models of High-Speed RLC Interconnect Delay for Complex and Real Poles-FEB 2017
- 29) Two-Extra-Column Trellis Min–Max Decoder Architecture for Nonbinary LDPC Codes-JAN 2017
- 30) - 010
- 31) Low power-delay-product dynamic CMOS circuit design techniques-MAR 2017
- 32) A Statistical Design Approach Using Fixed and Variable Width Trans conductors for Positive-Feedback Gain-Enhancement OTAs-FEB 2017
- 33) Novel Radiation-Hardened-by-Design (RHBD) 12T Memory Cell for Aerospace Applications in Nanoscale CMOS Technology-JAN 2017

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34) 28-nm Latch-Type Sense Amplifier Modification for Coupling Suppression-JAN 2017

35) High-performance engineered gate transistor-based compact digital circuits-FEB 2017

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