Multi-Objective Dynamic Voltage Restorer with Modified EPLL Control and Optimized PI Controller Gains

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Abstract—This paper describes a control algorithm based on Modified Enhanced Phase Locked Loop (MEPLL) in Dynamic Voltage Restorer (DVR). It compensates distortions and unbalances in the supply voltage along with voltage sag/swell. Three-phase MEPLL extracts the fundamental positive, negative and zero sequence components from the distorted/unbalanced signals. Further fundamental positive sequence components are used in the reference load voltage calculations. In addition to track the angle of the input signals similar to conventional phase-locked loops, the proposed algorithm (MEPLL) offers features of getting fundamental and sequential components in case of distorted or unbalanced grid voltage for all the three phases simultaneously. Optimization approach named as autonomous groups particle swarm optimization (AGPSO), a variant of PSO is used for calculation of PI controller gains. The Integrated Time Square Error (ITSE) is used as a cost function for optimization of an error between the reference and actual values. This approach of tuning PI gains improves the performance by eliminating the manual process. The proposed control algorithm is implemented in DVR system using MATLAB software and validated in a laboratory environment. The performance shows that the proposed control algorithm gives time effective and satisfactory solution for the unpredictable issues mentioned.

Index Terms—Sequence Components, Distortion, PI tuning, ITSE, Quadrature compensation, Sag.

I. INTRODUCTION

A Consumer expects reliable and qualitative power delivery at their load centers[1]. Moreover, it is not possible to supply constant power for the generating system at all the times due to power quality issues. Due to the exponential increase of power consumers having various non-linear loads, it is essential to study the power quality issues at the distribution level [2]. Mostly the power quality issues related to voltage variations like harmonics, sag, swell, imbalance, flickering, notches, fluctuations, and outages take place at the point of common coupling (PCC) where the other loads are also connected. Out of all these mentioned issues, some of the frequently occurring issues like voltage sag, swell, distortion and imbalance can be compensated by Dynamic Voltage Restorer (DVR) [3, 4]. DVR is a series connected Custom Power Device (CPD), which protects the critical, or sensitive loads from the aforesaid issues imposed by the supply source [5]. Its Basic operation and converter ratings depend upon type of compensation method, which includes in-phase compensation, quadrature compensation and pre-sag compensation [6]. The quadrature compensation method is preferred due to its advantage like zero active power requirement ideally as it compensates the voltage in perpendicular to the load current. It can replace the energy storage system with self-supported DC-bus further reducing the cost of energy storage system [7]. DVR is useful in single-phase and three-phase system to reduce voltage based power quality problems.

Several topologies and control algorithms for the DVR connected system has been studied in the literature [8-20]. Authors in [8-9] have used the cascaded inverter, H-bridge inverter based topologies in DVR system for the power quality improvement. Takushi et al. [10], has proposed a control method superimposing a zero-sequence component on the three-phase compensating voltages in shunt converter topology of DVR, which reduce the required ratings of the series converter and the series transformer by 50%, as compared to conventional method. Ebromah et al.[11] have explained the storageless DVR system based on three independent three-phase to single phase direct converters, in which the numbers of switches used are more as compared to the conventional topologies. Authors in [12], presented DVR composed of two conventional three-phase inverters series cascaded through an open-end winding transformer, where two equivalent implementations with either Level Shifted carriers PWM (LSPWM) or a Single Carrier PWM (SCPWM) strategy approaches were presented. Carlos et al.[13] have compared the three DVR topologies in compensation of voltage sags/swells in three-phase four-wire systems point of view under balanced and unbalanced conditions. The proposed systems use two independent DC links and presented the advantages in terms of switch blocking voltages and consequently lower DC bus voltage rating. The performance of DVR with selected topology depends upon control algorithm used for extraction of the reference voltage and generation of gating pulses for voltage source converter.
Authors in [14], have extended the steady-state analysis to transient analysis is proposed based on half cycle averaging, which can also eliminate the distortions in the supply side. A robust control scheme is used for medium voltage level DVR system for balanced and unbalanced sag [15], where the robustness specified by the selection of weighting functions and error tracking performance. In [16], three different configurations have been analyzed and it is observed that the DVR with a self-supported capacitor connected in shunt gives the best performance. Authors in [17], discussed the decomposition of voltages and currents in their sequences in the implementation of the open-loop control of a DVR. In literature [18, 19], Authors have discussed the characteristics of different single-phase and three-phase PLLs. These PLLs are responsible for controlling and synchronization of grid-connected converters. Another side, PLLs have characteristics for estimating the magnitude, phase, and frequency of power signals and so many industrial applications like measuring the harmonics, islanding detection of micro grids and welding industry etc. Authors in [20], have used the Software-PLL (SPLL) control strategy for compensating the power quality disturbances in the distribution system. However, LPFs used in SPLL are creating the delay and creating large variations in the DC bus voltage and terminal voltage. Authors in [21] proposed a control algorithm using the combination of enhanced phase lock loop (EPLL), where DVR was introduced as the effective solution for mitigating the voltage sag. The SRF-theory is revised for extracting Fundamental Positive Sequence Components (FPSCs) from the distorted signals in [22], where an algorithm based on SRF-theory has been developed for the generation of instantaneous reference compensating voltages for controlling a DVR. This novel algorithm makes use of the FPS phase voltages which were extracted by sensing only two unbalanced or distorted line voltages. In literature [23], a DSOGI pre-filter based PLL is employed to extract the symmetrical components of the grid voltage and eliminate the double frequency ripple from the estimated dq-voltages. The synchronization capability of three advanced synchronization systems, namely, Decoupled Double Synchronous Reference Frame-PLL (DDSRF-PLL), Dual Second Order Generalized Integrator-PLL (DSOGI-PLL), and three-phase enhanced-PLL (3p-EPLL) was studied in [24]. Authors in [25], proposed a fundamental sequence components (FSCs) extractor using third-order sinusoidal signal integrator based adaptive filters for effective synchronization of the DG system under distorted grid conditions. In [26], the review of the PLLs and the EPLL is presented comparing with conventional PLL. The advantages of modified EPLL which is implemented in this work over conventional EPLL like extracting and separating the sequence components (SCs) simultaneously for three-phase in a single unit are described in the literature [27]. Extraction of sequence components is essential for design of control algorithm for DVR. The proportional integral (PI) controller is one of the important components for regulating error components in the internal structure of control algorithm. Tuning of PI gains is another important task in such applications. Several design methods have been reported in literature for estimation of PI controller gains [28-30]. Most of them are algebraic formulas based classical methods which have been producing the result after certain limits of design parameters assumptions and work experience. These methods works based on the primary approximation and also consequent approximations/steps are unpredictable. So in this type of techniques, the error may be increased or decreased arbitrarily at any stage. Moreover, in the optimization based method for PI gain tuning, the random approximation is done at initial stage and then it converges to minimum value as errors are regulated in consequent approximations. Therefore, the optimization based method is one of effective solution for the estimation of PI gains [31-33]. A new version of Particle Swarm Optimization (PSO) named as Autonomous Groups PSO (AGPSO) algorithm is reported in the literature [34]. In this reference, AGPSO has been compared with basic PSO as well as recent modifications and it has merit compared to all variants in terms of trapping avoidance in local minima and convergence speed, particularly for problems of higher dimensionality. It is also clear that dividing particles in groups and allowing them to have different individual and social behavior can improve the performance of PSO significantly without extra computational burden. The different strategies have been used for updating the parameters of the algorithms and it is shown that AGPSO providing satisfactory performance compared to remaining PSO variations in engineering application.

In this paper, a new control algorithm based on Modified EPLL (MEPLL) is proposed for the three-phase DVR. All the possible voltage related power quality issues like sag, swell, distortions and unbalances are involved in the supply of DVR system. The impact of negative sequence component extraction is more dominant in case of the distorted or unbalanced source voltage. The advantage of MEPLL is that the simultaneous extraction of positive, negative and zero sequence components from the given distorted or unbalanced signals by taking the feedback of negative and zero sequences into account. In addition to that, a normal PI controller tuning process will take considerable time for exact tuning of its parameters. To overcome these issues, AGPSO the variant of PSO algorithm is used for PI controller gains tuning, as it is simple and basic of all the meta-heuristic optimization algorithms. The comparative performance of AGPSO is evaluated with basic PSO and with MPSO (Modified PSO), Time-varying Acceleration Coefficients PSO (TACPSO) as its recent variations.

II. SYSTEM DESCRIPTION AND DESIGN

Fig. 1(a) shows the complete diagram of DVR connected system which includes non-ideal AC grid, critical/sensitive loads, DC bus capacitor, voltage source converter (VSC), filter and injection-transformer. These main blocks along with the control block are shown in the figure. Supply voltage \(v_{abc}\) is measured at the point of common coupling (PCC) after considering the effect of source impedance \(Z_{abc}\) to see the real-time performance. The load voltages \(v_{labc}\) and load currents \(i_{labc}\) are sensed at the load bus where the critical load is being connected. The DC bus capacitor \(C_{dc}\) is chosen such that it can react to dynamical changes in the system spontaneously. The VSC converts DC to AC voltage with the help of gate pulses generated by the control algorithm. The
filter used here is to cancel-out the switching harmonics generated from the VSC and supply harmonics free voltage to the line. Fig. 1(b) describes the working operation of DVR principle in case of sag in supply voltage. During the sag condition, even though the magnitude of the source voltage of phase ‘a’ is $v_{sa}$ and that of the load voltage ($v_{La}$) is preserved to a pre-sag voltage ($v_{pre-sag}$) by the vectorial addition of ($v_{sa}$) and injected voltage ($v_{ca}$) as shown in Fig. 1(b). Pre-sag voltage ($v_{pre-sag}$) is defined as the magnitude of the system voltage before any disturbance.

![Fig. 1. (a) Block diagram of DVR system (b) Phasor diagram of DVR principle of operation](image)

### Design of the DVR system

Commences from system parameters like nominal voltage, frequency and kVA rating of the load taken into account. In sequence, it incorporates the design of primary objectives like turns ratio ($n$) and rating of injection-transformer, a DC bus capacitor ($C_{dc}$), interfacing inductor ($L_f$), filter constants ($R_f$ and $C_f$) and rating of VSC [2]. Detailed design parameter of three legs DVR is given in Appendix.

#### A. Rating of Injection-Transformer

The injection-transformer is a three unit of single transformer in which converter side windings are connected in star and supply side each winding connected in series with each line as shown in Fig.1 (a). The rating of the injection-transformer selected by the quantity of voltage is to be injected into the line during the dynamics. Let ‘a’ be maximum p.u. sag calculated with load voltage ($v_L$) taken as a base eqn.(1).Then the injected voltage ($v_{inj}$) is measured from eqn. (2), which is equivalent to transformer primary voltage. The load current calculated from eqn. (3) is used to compute the kVA rating of the transformer from the eqn.(4).

$$a = \frac{v}{v_L}$$  
$$v_{inj} = v_p = v_{L} \sqrt{1-a^2}$$  
$$\sqrt{3}v_Li_L / 1000 = kVA_{load}$$  
$$S = 3v_p i_L / 1000$$

#### B. Rating of VSC and DC Bus Capacitor

The voltage rating of VSC is chosen such that it should be capable of supplying the adequate voltage to the injection transformer i.e. $v_c = v_{sa}$. The current rating is chosen equal to load current i.e. $i_c = i_L$. The kVA rating of VSC is measured from the eqn. (5). The capacitor voltage is selected by the eqn. (6). The rating of the capacitor is selected based on the transient energy needed during the dynamics in source side. Expecting the energy stored in the DC bus capacitor ($C_{dc}$) is meeting the energy required by the load for the short duration of time ($\Delta t$) and it is measured by eqn. (7) where $V_{dc}$ is the DC bus voltage, $\Delta V_{dc}$ is the maximum change allowed in the DC bus voltage while transients were dealing.

$$kVA_{VSC} = \sqrt{3}v_i/1000$$

#### C. Interfacing Inductor ($L_f$) and Ripple Filter ($R_f$, $C_f$)

Interfacing inductor ($L_f$) is selected based on the maximum current ripple ($\Delta i_L$) allowed in the inductor. It is calculated from eqn. (8), where ‘$k$’ turns ratio of injection transformer, ‘m’ is modulation index, ‘$a$’ is overloading factor, and ‘$f$’ is switching frequency.

$$L_f = \frac{k \times (\sqrt{3/2}) \times m \times V_{dc}}{6 \times a \times f \times \Delta i_L}$$

A ripple filter contains capacitor ($C_f$), resistor ($R_f$) in series and they were estimated from Eqn. (9) as,

$$X_c = 1/(2 \pi f C_f)$$

### III. CONTROL SYSTEM

This section describes the proposed MEPLL based control algorithm for three-phase DVR. It is used for generation of three phase reference voltage. These reference voltages are used for generation of gating signals of VSC used as DVR. Mathematical analysis of control algorithm is presented to show the extraction of sequence components and to decide the control parameters of the algorithm. Normal proportional integral (PI) controller tuning process will take considerable time for exact tuning of its parameters. To overcome these issues, AGPSO, a variant of PSO, a meta-heuristic optimization algorithm is modeled for tuning the PI controller gains. Stability analysis of control algorithm followed by Optimization of PI controller is also discussed in this section.
A. Mathematical Description of MEPLL

The dotted portion in Fig. 2 depicts the MEPLL block in which it comprises of three phases simultaneously. It shows three subsections for three sequence components such as positive, negative and zero sequence components. The variables $V_1$, $w_1$, $\psi_1$, $V_2$, $\psi_2$, $V_0$, and $\psi_0$ represent magnitude, frequency, and phase of sequence components respectively. Now the mathematical analysis of MEPLL is given below. The simultaneous errors of three phases, which further processed in control algorithm is measured as in the eqn. (10).

$$e_{abc} = u_{abc} - y_{abc}$$

Where, $u_{abc} = v_{abc}$; $y_{abc} = y_{labc} + y_{2abc} + y_{0abc}$; $y_{labc} = V_1^* S(\psi_1)$; $y_{2abc} = -V_2^* S(-\psi_2)$; $y_{labc} = V_0^* S(\psi_0)$ and $S$ and $C$ are the vectors defined as,

$$S(\psi) = \begin{bmatrix} \sin(\psi) & \sin(\psi + \frac{2\pi}{3}) & \sin(\psi + \frac{4\pi}{3}) \end{bmatrix}^T$$

$$C(\psi) = \begin{bmatrix} \cos(\psi) & \cos(\psi + \frac{2\pi}{3}) & \cos(\psi + \frac{4\pi}{3}) \end{bmatrix}^T$$

And now by taking input signal $u = V^* S(\psi)$, the internal components of MEPLL, $z_i$ and $x_i (i=1, 2, 0)$ are estimated as,

$$z_1 = e_{abc}^S S(\psi_1) = \left[ V^* S(\psi_1) - V_1 S(\psi_1) - V_2 S(\psi_1) - V_0 S(\psi_0) \right] \times S(\psi_1)$$

Eqn. (14) can be simplified further as follows,

$$z_1 = \frac{3}{2} \left[ V^* \cos(\psi - \psi_1) - V_1 \cos(\psi_2 + \psi_1) \right]$$

Similarly

$$x_1 = e_{abc}^C C(\psi_1) = \frac{3}{2} \left[ V^* \sin(\psi - \psi_1) - V_1 \sin(\psi_1 + \psi_2) \right]$$

$$z_2 = e_{abc}^S S(\psi_2) = \frac{3}{2} \left[ -V^* \cos(\psi + \psi_2) - V_2 \cos(\psi_1 + \psi_2) \right]$$

$$x_2 = e_{abc}^C C(\psi_2) = \frac{3}{2} \left[ V^* \sin(\psi + \psi_2) - V_2 \sin(\psi_1 + \psi_2) \right]$$

$$z_0 = e_{abc}^S S(\psi_0) = \frac{3}{2} \left[ V_0 \cos(2\psi_0) - V_0 \right]$$
x_0 = e^{\psi_s} C(\psi) = \frac{3}{2} \left[ V_o * \sin(2\psi_o) \right]

(20)

Steady state error estimation in phase will be zero in the steady state condition i.e. \( (\psi - \psi_t) \approx 0 \)

\( \sin(\psi - \psi_t) \approx (\psi - \psi_t) ; \cos(\psi - \psi_t) \approx 1 \). In turn from the eqns. (14) to eqn. (20), by ignoring the double frequency terms, constant 3/2, eqn. (13) is modified as,

\[
\begin{align*}
\dot{V} = c_1 e^{\psi_s} S(\psi_t) = c_1 (V - V_c) \quad &\text{for all } \psi_t = \psi_c \\
\dot{V}_o = c_2 e^{\psi_s} S(\psi) = c_2 (-V_c) \\
\psi_2 = \psi_0 - \frac{c_1}{V} e^{\psi_s} C(\psi) = c_2 (\psi - \psi_t)
\end{align*}
\]

By applying Laplace transforms to the eqn. (21) transfer functions for magnitude and phase are derived as given in eqn. (22).

\[
\begin{align*}
V_2(s) &= \frac{c_2}{s^2 + c_2 s + c_3} \\
\psi_2(s) &= \frac{c_2}{s^2 + c_2 s + c_3} \psi_0(s)
\end{align*}
\]

(22)

From the polynomial in the eqn. (23), it is clear that \( c_2 \) and \( c_3 \) are the control parameters in this algorithm. For estimating these internal parameters of MEPLL, the characteristic equation given in eqn. (23) is utilized for the stability analysis which is reported in the next subsection.

B. Stability Analysis of MEPLL

The open loop transfer function comprises controlling parameters \( c_2 \) and \( c_3 \). These are obtained from a characteristic polynomial of eqn. (23) as,

\[
G(s) = \frac{c_2 s + c_3}{s^2 + c_2 s + c_3}
\]

(24)

Where \( k = c_3 \) and \( T = \frac{c_2}{c_3} \); Therefore \( \omega = \frac{T}{c_2} \) is the corner frequency. The Bode plot for stability criteria is used for finding the control parameters \( (c_1, c_2) \). Fig. 3 shows the corresponding Bode plot for three transfer functions G1, G2 and G3 with three combinations of gain \( (k) \) and frequency \( (\omega) \).

The detailed analysis of Fig. 3 is given in Table-I. Three cases were compared by the varying gain \( (k) \) and frequency \( (\omega) \). In the first two cases \( k \) is kept constant and \( \omega \) is varied and in last two cases, \( \omega \) is kept constant and \( k \) is varied. Even though the phase margin (PM) is same for both the first case and third case, the third case is selected as a suitable one because of the higher distance between gain crossover frequency \( (\omega_{gc}) \) and phase crossover frequency \( (\omega_{Ph}) \) i.e. \( \omega_{gc} < \omega_{Ph} \) which ensures the system to be stable. Thus \( c_2, c_3 \) variables have been selected based on the third case in Table-I.

The gains \( c_1, c_4, \) and \( c_6 \) are identical because the division block is used to have the magnitude independent. The gains \( c_1, c_2, \) and \( c_3 \) are also identical. Moreover, the gains \( c_1, c_2 \) and \( c_6 \) are being made equal to simplify the estimation of parameters. After selecting the controlling parameters, the value of \( c_2 \) and \( c_3 \) are found to be 10 and 100 respectively. The values of \( c_1, c_4, \) and \( c_6 \) are kept at 10 each as \( c_1 \) and \( c_2 \) are made equal. Another side, the values of \( c_5 \) and \( c_7 \) are kept at 100 each as for mathematical simplicity.

C. Optimization of PI Tuning

For exact estimation of parameters of PI controller, AGPSO, the variant of meta-heuristic PSO algorithm is proposed which is simple in design and more accurate. Four variables namely DC-PI controller gains \((k_{p1}, k_{i1})\) and terminal voltage-PI controller gains \((k_{p2}, k_{i2})\) are to be optimized. As shown in Table-II, AGPSO updates learning factors \( b_1 \) and \( b_2 \) in four groups. The proposed optimization algorithm starts the procedure with a random selection of initial positions for search agents and their positions will be updated in each iteration till the maximum iteration \((max_it)\). The dimension \((dim)\) of the search space is same as the number of variables to be optimized. After so many trials, the lower \((lb)\) and upper \((ub)\) bounds were fixed between 0 and 30 respectively. Similarly, the number of search agents \((nop)\), maximum iteration \((max_it)\) are selected as 20 and 10 respectively. The cost function \( F_{cost} \) selected for this algorithm is Integrated Time Square Error (ITSE) as given in the eqn. (25). Its aim is to compute the PI gains by converging the error between the reference and actual values towards zero.

\[
F_{cost} = \int t e^2(t) dt
\]

(25)

Fig. (4) Shows the flowchart of the optimization algorithm for finding PI controller gains, where ‘t’ represents the current iteration. This algorithm starts with initializing its all parameters and position \( (x) \) for all the search agents randomly. Here velocity, ‘v’ and position, ‘x’ of search agents are to be computed by using eqn. (27) and eqn. (28) respectively.
for every search agent MATLAB model of DVR system gets simulated and the cost function \( F_{cost} \) to be updated.

\[
\begin{align*}
\text{START} \\
\text{Initialize all parameters} \\
\text{and variables (kp1, k1, kp2 and k2)} \\
\text{Initial positions of} \\
\text{variables} \\
\text{Compute v and x} \\
\text{\( i = \text{max it} \) } \\
\text{Compute \( F_{cost} \) and simulate} \\
\text{MATLAB model for each} \\
\text{search agent} \\
\text{Update \( P_{best} \) according to} \\
\text{Gbest fitness value} \\
\text{Calculate new position} \\
\text{and velocity of search agents using eqns (21, 28)} \\
\text{STOP} \\
\end{align*}
\]

During this process two positions \( P_{best} \) and \( G_{best} \) to be stored at every iteration, former is for the best position in particular iteration and later one is for best position out of all the iteration as on that iteration.

\[
w = w_{\text{max}} - n \left( \frac{w_{\text{max}} - w_{\text{min}}}{\text{max it}} \right) \tag{26}
\]

\[
v_{\text{id}}^{n+1} = w \times v_{\text{id}}^n + b_1 \text{rand()} \times (p_{\text{id}}^n - x_{\text{id}}^n) + b_2 \text{rand()} \times (g_{\text{id}}^n - x_{\text{id}}^n) \tag{27}
\]

\[
x_{\text{id}}^{n+1} = x_{\text{id}}^n + v_{\text{id}}^{n+1} \tag{28}
\]

Where \( 'w' \) represents inertia weight which is updated for every iteration using the eqn. (26), \( 'n' \) is a current iteration, \( '\text{max it}' \) maximum iterations, \( 'i' \) is an \( i^{th} \) particle, \( 'd' \) is the dimension of the variable, and \( b_1, b_2 \) are the learning factors. The proposed algorithm AGPSO is further changing the diversity of particles[34].

### D. Estimation of Reference Load Voltage and Gate Pulse Generation

The fundamental positive sequence of the three phase source voltage \( (v_{\text{abc}}) \) is obtained from MEPLL. It consists of three phase voltage such as \( v_{\text{a}}, v_{\text{b}}, v_{\text{c}} \). The in-phase and quadrature unit templates are calculated from sensed three phase load currents as[2],

\[
u_p = \frac{i_a^p}{i_m}; u_{ph} = \frac{i_b^p}{i_m}; u_{pc} = \frac{i_c^p}{i_m} \tag{29}
\]

\[
u_p = \frac{3u_{ph} + u_{pc} - u_{pc}}{2\sqrt{3}}; u_p = \frac{-3u_{ph} + u_{pc} - u_{pc}}{2\sqrt{3}} \tag{30}
\]

Where \( i_m = \frac{2}{3}(i_a^p + i_b^p + i_c^p) \)

Thus, in-phase and quadrature unit templates are calculated from eqn. (29) and eqn. (30) by taking load current \( (i_{\text{abc}}) \) as its sensed input. The output of DC-PI controller \( (v_{\text{dcp}}) \) is multiplied with in-phase unit templates \( (u_{\text{abc}}) \) to calculate component \( (v_{\text{abc}}) \) from the eqn. (31). The load voltage amplitude \( (V_1) \) is computed from sensed three phase load voltage \( (V_{\text{abc}}) \) [2]. The reference load voltage magnitude \( (V_*) \) is compared with actual computed terminal voltage amplitude \( (V_1) \) and extracted voltage error \( (V_\text{e}) \) has been given to PI controller. The output of AC-PI controller \( (v_{\text{abc}}) \) is multiplied with quadrature unit templates \( (u_{\text{abc}}) \) thus obtaining component \( (v_{\text{abc}}) \) from eqn. (32).

\[
\begin{align*}
V_{pa} &= V_{dcp}u_{pa}; V_{pb} = V_{dcp}u_{pb}; V_{pc} = V_{dcp}u_{pc} \tag{31} \\
V_{qa} &= V_{dcp}u_{qa}; V_{qb} = V_{dcp}u_{qb}; V_{qc} = V_{dcp}u_{qc} \tag{32}
\end{align*}
\]

Reference load voltages for phase ‘a’, phase ‘b’ and phase ‘c’ \( (v_1, v_{\text{abc}}, v_{\text{abc}}) \) are estimated using extracted value of positive sequence voltages \( (v_{\text{abc}}, v_{\text{abc}}, v_{\text{abc}}) \) and estimated value of voltage components from eqn. (31) and eqn. (32). It is given as,

\[
\begin{align*}
V_{La} &= v_{q1} + v_{q2} + v_{q3}; V_{Lb} = v_{q1} + v_{q2} - v_{q3}; V_{Lc} = v_{q1} - v_{q2} - v_{q3} \tag{33}
\end{align*}
\]

For simplicity, the phase ‘a’, phase ‘b’ and phase ‘c’ reference load voltages \( (v_1, v_{\text{abc}}, v_{\text{abc}}) \) are considered as \( v_{\text{abc}} \). Now for the gate pulses for IGBT’s of VSC, reference load voltages \( (v_{\text{abc}}) \) are compared with actual load voltage \( (V_{\text{abc}}) \) sensed and amplified magnitude of three phase error components are passed through a 10 kHz triangular wave for comparing as well as generating pulse width modulated (PWM) switching signals.

### IV. Simulation Results

The Simulink model of three-phase DVR with control algorithm is developed in MATLAB environment. The system performance is carried out using solver 23ib in variable step with a sample time of 20 µs. An effective study of the proposed control algorithm, simulation model of three-wire DVR system is executed for 2 second and within this range all the dynamics are provided in the source voltage within the execution time such as sag at 0.86 sec, swell at 0.98 sec, distortions at 1.1sec and imbalance at 1.2sec with a duration of three cycles each. The switching frequency used for generation of gating signal for IGBTs based VSC is 10 kHz. The parameters used in simulation work are presented in Appendix.

#### A. Performance of Control Algorithm

Fig. 5(a), depicts the distortion and unbalance in the input signals and elaborate the MEPLL’s application for extracting fundamental positive sequence components from the distorted and unbalanced supply source. The response of the intermediate signals of MEPLL such as \( x_1, z_1 \) and \( V_1 \) are
depicted in this figure. The negative ($y_{abc}$) and zero sequences ($y_{abc}$) components are also shown in Fig.5 (a). The positive sequence components ($y_{abc}$) signal of MPELL is same as the fundamental positive sequence ($v_{eq}$) components of the supply voltage ($v_{abc}$) as shown in Fig. 5(b). The load reference voltage ($v_{Lref}$) is estimated by using eqn.(33) for phase ‘a’, phase ‘b’ and phase ‘c’. Finally, the actual load voltage ($v_{Labc}$) is presented to compare it with the reference load voltage ($v_{Lref}$). The required reference load voltage ($v_{Lref}$) is obtained according to the desired magnitude of load voltage, which further helps in generating gate pulses for the VSC used in DVR for compensating the disturbances in the supply voltage.

![Figure 5](image)

Fig. 5. (a) Extraction of Sequence components from distorted and unbalanced signal (b) Generation of reference load voltage.

### B. Performance of DVR under Sag, Swell, Distortion, and Imbalance

To investigate the performance of control algorithm on three phase DVR under sag, swell, distortion and imbalance in AC mains, simulation work is carried out and results are presented. The sag of 0.1 p.u, swell of 0.2 p.u, and distortion are created by appending 5th and 7th harmonics with the magnitude of $1/5^th$ and $1/7^th$ of fundamental voltage and imbalance is created by connecting a resistive load in between the two phases. In Fig. 6, Phase to phase voltage of source ($v_{s}$) with sag, swell, distortion and imbalances are shown at the timing instants (t) of 0.86sec, 0.98sec, 1.1sec and 1.2sec respectively. At the same instants, it can be seen that three phase DVR voltages ($v_{va}$, $v_{vb}$ and $v_{vc}$)injeting suitable magnitude of voltage so that the load voltage ($v_{l}$) is maintained stiff at the required magnitude. The load current ($i_{l}$) can be observed without any disturbances during the timings of disturbances at the source side. The dynamic response of DC-bus voltage ($v_{dc}$) can be depicted in the same figure.

![Figure 6](image)

Fig.6. Performance of DVR under sag, swell, distortion and unbalance

### C. Optimization of Gains of PI-Controller

The optimization algorithm is used for tuning of DC bus PI controller and terminal voltage PI controller gains. The comparison of proposed AGPSO based optimization algorithm with PSO and its variations are presented here. From the Fig. 7, the variation of the convergence curve for the cost function with respect to iterations can be observed. It can be seen from the same figure that, the cost function AGPSO comes towards the steady-state value within 6 iterations. It means that the convergence curve is converging very fast for the given cost function by using AGPSO algorithm. The variations of $k_{p}$, $k_{i}$ values of both the PI controller for each iteration can also be observed in Fig. 8. Fig.8 (a-b) shows the variation of PI gains ($k_{p}$, $k_{i}$) values with respect to each iteration of AGPSO algorithms for DC bus PI and terminal PI controllers respectively. In both the figures, the left y-axis shows the variation of $k_{p}$ and right y-axis shows the variation of $k_{i}$ with respect to iterations. The detailed list of all the parameters of all the four optimization algorithms are mentioned in Table-II. To observe the execution of PI controller with optimization algorithms, the DC bus PI tuning is presented with voltage sag dynamics at 0.5s to 0.6s and it is shown in Fig. 9(a). The expanded view of the waveform is given in Fig. 9(b). This Figure shows the clear picture of variation of the four PSO algorithms and it can be observed that, the AGPSO is making DC bus stable faster as compared to others. As it is an underdamped system, rise time ($T_{r}$) is calculated at 100% of final value (i.e. at 300 V) and settling time ($T_{s}$) is calculated.
for 2% of tolerance band (i.e. 294-306 V). The details of the zoomed figure are given in Table-III.

**D. Harmonic Analysis**

The total harmonic distortion (THD) in the distorted source voltage ($v_{sa}$), load voltage ($v_{la}$) and load current ($i_{la}$) of phase ‘a’ are analyzed and shown in Fig.10. The level of distortions in supply voltage was created by injection of the extra harmonic source. So, the measured THD in source voltage ($v_{sa}$) is 28.88% with fundamental RMS voltage of 406.7V as shown in Fig.10(a) where load voltage ($v_{la}$) is found 3.49% of THD with fundamental RMS voltage of 415.35 V (587.4/1.4142) as shown in Fig.10(b). After compensation, the THD of the load current is 0.81% with 13.92 A as it can be observed in Fig.10(c). At the end of this study, it is observed that DVR with developed control is able to compensate distortion within 5% according to IEEE-519-2014 guideline.

![Convergence curve](image1)

**Fig.7. Convergence curves**

![Variations of k_p, k_i](image2)

**Fig.8. Variations of k_p, k_i throughout the iterative process of AGPSO in case of (a) DC-PI (b) AC-PI**

**TABLE-II: DETAILED COMPARISON OF OPTIMIZATION ALGORITHMS IN PI TUNING**

<table>
<thead>
<tr>
<th>Sr. No</th>
<th>Algorithm</th>
<th>Cost function value</th>
<th>Minimum No. of iterations taken to settle cost function</th>
<th>DC bus PI controller</th>
<th>Terminal voltage PI controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>PSO</td>
<td>31.30</td>
<td>7</td>
<td>9.52</td>
<td>0.29</td>
</tr>
<tr>
<td>2.</td>
<td>MPSO</td>
<td>31.74</td>
<td>7</td>
<td>10.00</td>
<td>1.25</td>
</tr>
<tr>
<td>3.</td>
<td>TACPSO</td>
<td>30.22</td>
<td>10</td>
<td>10.60</td>
<td>0.33</td>
</tr>
<tr>
<td>4.</td>
<td>AGPSO</td>
<td>30.24</td>
<td>6</td>
<td>12.38</td>
<td>0.21</td>
</tr>
</tbody>
</table>

![Harmonic Spectra](image3)

**Fig. 10. Harmonic Spectra of (a) distorted supply voltage (b) load voltage and (c) load current of phase ‘a’**

**TABLE-III: DYNAMIC PARAMETERS OF FIGURE 9(B)**

<table>
<thead>
<tr>
<th>Sr.No</th>
<th>Used Algorithm</th>
<th>Peak magnitude, M_p(%)</th>
<th>Rise Time, T_r(sec)</th>
<th>Settle Time, T_s(sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>PSO</td>
<td>4.3</td>
<td>0.105</td>
<td>0.132</td>
</tr>
<tr>
<td>2.</td>
<td>MPSO</td>
<td>5.5</td>
<td>0.095</td>
<td>0.168</td>
</tr>
<tr>
<td>3.</td>
<td>TACPSO</td>
<td>4.5</td>
<td>0.098</td>
<td>0.128</td>
</tr>
<tr>
<td>4.</td>
<td>AGPSO</td>
<td>2.6</td>
<td>0.065</td>
<td>0.072</td>
</tr>
</tbody>
</table>

![DC Link V-Ref](image4)

**Fig. 9. (a) Performance of algorithms in tuning DC bus Voltage and (b) its expanded view**
V. IMPLEMENTATION RESULTS

To validate the system performance, a prototype of three phase DVR is built in the laboratory environment. The proposed control algorithm (MEPLL) with an optimized PI controller is programmed in FPGA based XC3S5000 series processor in real time using OP-5142. A signal conditioning circuit is designed for sensing input voltage and current signals. Sensed input signals are needed for the control algorithm to generate the required gate signals for voltage source converter. The experimental results are recorded using 4-channel Digital Storage Oscilloscope -DSO-X-2004A and Fluke made single-phase power quality analyzer (43B). The steady-state performance is recorded using single-phase power quality analyzer during the distortions created in the AC mains, whereas dynamical results are captured by DSO during sag, swell, distortions and imbalance in same source voltage.

A. Performance of DVR using ‘MEPLL’ Control and Reference Voltage Generation

The control performance signals of MEPLL and reference voltage generation are shown in Fig. 11 (a-b). Fig. 11(a) shows the extraction of positive, negative and zero sequence components from a given distorted signal of phase ‘a’. As the line voltages of supply are measured, it shows RMS value of 423 V with a fundamental value of 406 V. The signals are given to MEPLL after converting line voltage into phase voltage, so the MEPLL is extracting all the signals in phase voltage values only i.e. positive sequence component (v<sub>1a</sub>) of 226.9 V (RMS), negative sequence component (v<sub>2a</sub>) of 6.2 V (RMS) and zero sequence component (v<sub>0a</sub>) of 7 V (RMS) respectively. Similarly in Fig. 11(b) shows the extraction of positive, negative and zero sequence components of a given unbalanced signal of phase ‘a’. Since three phases are unbalanced, phase ‘a’ voltage (line-line) comes out to be 373 V (RMS), positive sequence component of phase ‘a’ (v<sub>1a</sub>) is 222 V of phase RMS, negative sequence component of phase ‘a’ (v<sub>2a</sub>) is 34.3 V of phase RMS and finally zero sequence component of phase ‘a’ (v<sub>0a</sub>) is 4.6 V phase RMS. Fig. 12 (a-b) shows the generation of the reference source voltage from the fundamental positive sequence component of a source voltage (v<sub>sf1a</sub>) of phase ‘a’. It includes the elements (v<sub>da</sub>) and (v<sub>qa</sub>) which are obtained by multiplying the DC-PI controller output with an in-phase unit template (u<sub>pa</sub>) and AC-PI controller output with quadrature unit template (u<sub>qa</sub>) respectively. Fig. 12(a) shows, the source voltage (v<sub>sf1a</sub>) of phase ‘a’ with distortion free of 233 V value, 242 V value of reference load voltage (v<sup>*</sup><sub>La</sub>) of phase ‘a’ is generated after addition and subtraction of 14.1 V of v<sub>da</sub> and 3.9 V of v<sub>qa</sub> respectively. Fig. 12(b) shows, the source voltage (v<sub>sf1a</sub>) of phase ‘a’ imbalance with 227 V RMS value, 240 V RMS value of reference load voltage (v<sup>*</sup><sub>La</sub>) of phase ‘a’ generated after addition and subtraction of 28.1 V of v<sub>da</sub> and 5.2 V of v<sub>qa</sub> respectively. In all the cases the reference voltage value comes out to be exactly 240 V phase value which is equivalent to 415 V line value after compensation.

B. Dynamic Performance of DVR

Fig. 13(a-c) and Fig. 14(a-c) show the dynamic performance of three-phase DVR under distortion and unbalanced AC mains respectively. Fig. 13(a) and Fig. 14(a) are the source voltages (v<sub>sabc</sub>) with the line RMS voltage of 415 V and 390V under supply voltage is distorted and unbalanced respectively. Fig. 13(b) and Fig. 14(b) are the injected voltage (v<sub>cabc</sub>) of source voltages (v<sub>sabc</sub>) of phase ‘a’. Fig. 13(c) and Fig. 14(c) are the load voltages (v<sub>Lref</sub>) with line RMS voltage of 415 V and 390V under supply voltage is distorted and unbalanced respectively.
DVR in distortion and unbalance cases respectively. Fig. 13(c) and Fig. 14(c) shows the compensated load voltage ($v_{Labc}$) with the RMS line voltage of 414 V and 414 V when the supply voltage is distorted and unbalanced respectively. In all the cases DC bus voltage ($V_{dc}$) is shown with a small variation from 300 V. From above discussion, it is clearly seen that the DC bus voltage is maintained at its reference level with small variation while dynamics occurred in the supply voltage. However, the dynamic response of the DVR using MEPLL control algorithm with voltage sag, voltage swell, distortions, and unbalance in the supply is given in Table-IV.

C. Steady State performance of DVR

Steady-state performance of DVR is depicted by measuring THD of the distorted source voltage ($v_{sa}$), load voltage ($v_{La}$) and load current ($i_{La}$) of phase ‘a’ and can be observed from Fig. 15. So, Distortion in source voltage ($v_{sa}$) can be seen in Fig. 15 (a) with fundamental RMS voltage of 406.7 V (total RMS 423 V) whereas Fig. 15 (d) shows the load voltage ($v_{La}$) is coming out with 2.4% with fundamental RMS voltage of 415 V and the THD of the load current is 0.9% with 13.9 A as shown in Fig.15 (e).

VI. CONCLUSIONS

The objective of this paper is to improve quality of supply power at the consumer side in case of sag, swell, distortion and imbalance in the supply voltage. The validation of the proposed control algorithm (MEPLL) is performed by comparison of system performance for all cases like sag, swell, distortion and imbalance in the supply voltage. The proposed control algorithm is dynamically responding to the power quality issues mentioned and it is efficiently extracting the sequence components from the distorted signals. The control algorithm is working effectively and producing the expected results within time, which helps in reducing the overall time of mitigating aforesaid problems. Furthermore, execution time is reduced by optimization algorithm proposed in tuning process of PI-controller gains. From the performance waveforms of PI tuning by AGPSO, it can be understood that the tuning speed of the PI-controller gains is improved from
the conventional tuning process. By using the MEPLL with AGPSO, the performance of the three-phase DVR is significantly improved. The limitation of this method is that, understanding of the MEPLL algorithm is challenging without clear mathematical analysis, however, it is useful in the applications where FSCs is required for internal processing. The future scope of work is that this algorithm can be utilized for the control of the distorted and unbalanced cases of distributed power generation systems like wind or solar.

APPENDIX

System parameters: Non-ideal Supply voltage-415 V, 50 Hz; Load of 10kVA with 0.8 p.f. (Lagging); v(s during sag)=0.7*240 =168 V; Load current ($i_L$)=13.91 A; Rating of injection-transformer=3*171.39*13.91/1000=7.152 MVA; Terminal voltage PI controller gains: $k_p^2=24.70$, $k_i^2=1.44$, $k_p^1=60$, $k_i^1=10$ MVA; Internal constants of MPDLL: $c_1=10$, $c_2=10$, $c_3=100$, $c_4=10$, $c_5=100$, $c_6=10$, and $c_7=100$, DC bus PI controller gains: $k_p^1=12.327$, $k_i^1=0.210$, Terminal voltage PI controller gains: $k_p^2=24.70$, $k_i^2=1.44$, Switching frequency ($f_s$) =10 kHz, Cut-off frequency of low pass filter at DC bus = 12Hz, Cut-off frequency of low pass filter at AC bus = 10Hz. Sampling time ($t_s$)=20 usec.

REFERENCES


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