Abstract—The control of a switched reluctance motor (SRM) drive is proposed with a front end power factor correction (PFC) converter. It uses a modified Cuk converter fed SRM drive to improve power quality at AC mains. The converter configuration consists of two Cuk converters and each of them operates separately for two half cycles of the supply voltage. The proposed converter generates two identical voltages across two output capacitors to feed a split capacitor converter of a 4-phase SRM drive. The proposed pulse width modulated AC-DC converter operates in discontinuous conduction mode (DCM) to reduce its size and cost by eliminating couple of sensor requirement. The incorporated voltage control loop regulates the DC link voltage to bring down the supply current THD under acceptable limits as well as passive filters are incorporated in the circuit, which reduce harmonics content from the input supply current, active shapers as they reduce the harmonics current content, which are at the frequency other than the fundamental frequency. To meet today’s demand, brushed and commutator based machines are no more the choice for industry because of associated wear, low power density and reliability. The brushless motors with permanent magnets, are becoming popular due to their high efficiency, however, the cost and availability of the rare earth permanent magnet material, are the limitations associated with these permanent magnet motors. Hence, the advent of SRM (Switched Reluctance Motor) has met the requirement of low cost variable speed drive motor. However, the simple construction and absence of rotor windings or any sort of rare earth material, have reduced the cost of SRM, effectively [2-4]. Moreover, SRM also suffers from some disadvantages including high torque ripple due to discontinuous phase current, acoustic noise, vibration etc. Thus, many online and offline controls are reported in the literature for torque ripple minimization in SRM to present SRM as an appliance motor. Sozer et al. [3], have given the calculation for commutation angle control on the basis of three control parameters i.e. peak phase current, angle when first current peak occurs and the angle when inductance begins to increase. Hussain [4] has presented the hybrid torque minimization controller incorporated torque minimization technique developed in the past few decades.

In this paper, SRM drive with an improved efficiency is proposed by reducing the switching devices of SRM converter. The paper compares the proposed split AC converter for SRM drive with a conventional converter having more switching devices on the basis of cost and efficiency. Moreover, poor power quality with high input current THD remains undiscussed. In [5], Chai et al. have proposed the three phase single switch mode rectifier fed SRM drive. The current harmonics cancellation scheme and voltage control scheme, are discussed in it. Test results have demonstrated enhanced current and speed dynamic responses with reduced vibration and speed ripples, however, power factor improvement has been still limited, which do not comply a standard. Many low cost SRM based drives are proposed in the literature but SRM drive with improved power quality is not well addressed till now.

The low cost switched reluctance motor drive fed by a unity power factor converter, appears as a promising solution to the available drive structure. The mid-point converter which utilizes single switch and single diode to excite individual phases, is selected here to build the proposed drive as a low cost system. This converter is well suited for inexpensive

I. INTRODUCTION

Power factor correction (PFC) converters are becoming popular due to their distinguished features of low input current THD (Total Harmonic Distortion) with a high power factor. These PFC converters are basically the input current shapers as they reduce the harmonics current content, which are at the frequency other than the fundamental frequency. To reduce harmonics content from the input supply current, active as well as passive filters are incorporated in the circuit, which bring down the supply current THD under acceptable limits as per the standard IEC 61000-3-2 [1]. To meet the demand of energy efficient, low cost variable speed drive is a fan type of load used in ventilation, air conditioning and dryer applications, a PFC converter based modified dual output Cuk converter fed SRM drive is proposed in this work.

The requirement of variable speed drive for household applications, has intensified the interest of manufacturers towards the low cost and highly efficient brushless motor drive.

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application due to reduced count of switches and drivers requirement. However, switch voltage rating requirement is half because of its split DC link configuration. The only drawback associated with this so far unpopular converter topology, is the required voltage symmetry. This encourages the design of PFC converter, which can take care of power quality issues at AC mains and generates two symmetrical voltages across the two capacitors. Therefore, a dual output Cuk converter fed SRM drive is proposed here. The selection of modified dual output Cuk converter is made because of following influential features.

- It provides a fully regulated two equal output voltages utilizing single voltage loop.
- It improves the power quality when the drive operates under steady state as well as dynamic conditions.
- The selected operating mode for proposed converter, has reduced the size of an output side inductor thus the cost and required board area, are also reduced.

To control SR motor, two control methodologies are adopted as a constant DC link voltage based control and a variable DC link voltage based control. The constant DC link voltage based control is the conventionally adopted control algorithm, which is further divided into two operating modes on the basis of operating speed. If the low speed operation is desired then the chopping control mode is adopted whereas a single pulse mode is selected at high speed operation. During low speed, the turn on and turn off angles are kept constant and the required torque is obtained by regulating amplitude of the current. However, during high speed operation, the current control is not possible due to comparable back EMF and DC link voltage. Therefore, SR motor at high speed is controlled on the basis of turn on and turn off angles which can be called as a single pulse mode control. In this conventional control method, full DC link voltage is applied across the winding during low speed operation, which results in high current gradient thus initializes the different vibration modes in the stator and produces increased acoustic noise. However, acoustic noise becomes prominent when the stator frequency of vibration coincides with the natural frequency of the stator. The high acoustic noise and radial vibrations in SRM, can be reduced using single pulse control, which is selected here. In this proposed control algorithm, the DC link voltage is considered as function of speed. The PFC converter before mid-point converter fed SR motor, provides required power quality improvement at supply side and at the same time it is capable of maintaining sufficient current to maintain the rated torque. Thus low speed operation of SR motor can be easily obtained without using any chopping control strategy. The reduced DC bus voltage at low speed operation, results in reduced current gradient and thus the acoustic noise as compared to conventional control method.

II. PRINCIPLE OF PFC TECHNIQUE

The switching control for PFC based converters, can be categorised as a variable frequency control and a constant frequency control [6-7]. The variable frequency control is generally based on output voltage ripple with constant-on-time (COT) or constant-off-time. Moreover, the converter operates with fixed duty cycle, however, at variable frequency, the converter switch turns on if the condition, $V_{\text{ref}} > V_{\text{dc}}$ is true, whereas $V_{\text{dc}}$ is the DC link voltage and $V_{\text{ref}}$ is the set reference voltage [8]. The pulse bursting phenomenon is the demerit associated with the COT (Constant on Time) control, i.e., the occurrence of very short off time pulse after COT pulse. Whereas, the constant frequency control is the pulse width modulation (PWM) based control, which are categorised as a voltage based control and a current based control.

The voltage based control with variable duty cycle, is proposed here. The continuous and discontinuous natures of the inductor current, decide the operating mode of PFC converter. On the basis of the current nature through the inductor, three operating modes are reported in the literature, i.e., continuous conduction mode (CCM), critical conduction mode (CRM) and discontinuous conduction mode (DCM) [8-9]. In CCM, the continuous inductor current results in low current ripple with reduced electromagnetic interference (EMI). However, the switch experiences hard switching as the current is continuous all the time. The CRM and DCM are preferred because the inductor current is discontinuous in every switching cycle, which allows the zero current switching [10]. The only difference in CRM and DCM modes, is that in CRM, one customizes the design for boundary condition to reduce peak current stress through the switch.

Figs. 1(a) and (b) represent the conventional Cuk converter in DCM of operation. However, Fig. 1(b) presents the output inductor current behaviour, during switch on period $D_1T$, as the inductor current increases and then it decreases to zero till switch off period $D_1T$, while the remaining period, $(1-(D_x + D_y))T$ of switching period, is the freewheeling period when the output inductor current freewheels through the circuit diode. To obtain inherent PFC, the duty cycle, $D_1$ is varied from zero to its maximum value for every half cycle of the supply voltage.

Fig. 1(a) Conventional Cuk converter and (b) Output inductor current during DCM of operation.
III. MODIFIED DUAL OUTPUT CUK CONVERTER FED SRM DRIVE

The proposed PFC converter fed SRM drive is shown in Fig. 2. The need for a dual output, arises as a special split capacitor converter configuration is used, such that each phase is connected through a single switch and one diode to drive a SRM. The converter circuit comprises of two Cuk converters with one common switch and featured with two output voltages equal in magnitude. This converter topology is derived from PFC based three phase rectifier topology first proposed in [11]. The proposed converter consists of single input inductor operating in CCM to reduce input current ripple. The other circuit components include intermediate capacitors, output side inductors and output capacitors. This configuration has added advantage of self-balanced output voltages without any required complex control for voltage balancing. The balanced output voltages have reduced the sensor cost, as while sensing output voltage across one output capacitor gives total DC link voltage. The sensed DC link voltage is compared with reference DC voltage to generate switching pulses for the converter.

IV. OPERATION OF MODIFIED CUK CONVERTER

The converter operation is divided into two half cycles i.e. negative half and positive half of the input voltage waveforms. Two intermediate capacitors, C1 and C2 and output inductors L_{o1} and L_{o2} are introduced in the circuit. The input side inductor L_i operates in continuous current mode (CCM) and output inductors L_{o1} and L_{o2} are allowed to enter discontinuous conduction mode (DCM) during each cycle of operation, which is shown in Fig. 3. The energy transfer between passive elements in the circuit, can be explained under five different modes of operation.

- **Mode I (During positive half cycle switch on period t=0-t_1):** During this time interval, positive half cycle is shown in Fig. 4(a). This mode presents the energy flow from mains to inductor L_i through diodes D_1 and D_2. The switch on state, is described in this mode during positive half cycle. The charging current for inductor, L_{o1} passes through through the switch and output side capacitor C_{dc1}. However, intermediate capacitor is discharged during this mode.

- **Mode II (During positive half switch off period t_1-t_2):** In the previous mode, capacitor C_1 is left discharged, which is charged from the inductor current i_{L_i}. It finds its path through diodes D_1, D_4 and D_3 as shown in Fig. 4(b). The output side inductor L_{o1}, which is charged during Mode-I, is discharged through a capacitor, C_{dc2} during this mode. This mode ends with fully charged output capacitor C_{dc2}.

- **Mode III (DCM Mode t_2-t_3):** Fig. 4(c) shows the circuit operation during this time interval. The output inductor current decreases below zero during this operation mode. During this mode, the converter circuit appears as emulated resistance, which allows constant circuit current.

- **Mode IV (During negative half switch on period t_3-t_4):** During this time interval, a negative half cycle is associated with converter operation. This mode is shown in Fig. 4(d). This mode describes the switch on period, inductor L_i stores energy, the switch on state, provides the path for input inductor current and the current is flowing through intermediate capacitor C_1 and inductor L_{o2}. The output side capacitor, C_{dc2} is charged during this mode. Moreover, the input inductor current finds its path through diodes D_2 and D_3.

- **Mode V (During negative half switch off period t_3-t_4):** The stored energy in L_i during Mode V is transferred to intermediate capacitor C_2. Moreover, diodes D_2, D_3 and D_3 provide path for capacitor charging current. The inductor L_{o2} transfers its energy to output side capacitor, C_{dc2} through diodes D_2 and D_3. The flow of current during this interval, is displayed in Fig. 4(e).

- **Mode VI (DCM mode t_4-t_5):** Fig. 4(f) shows the DCM with zero output inductor current during negative half cycle.
V. DESIGN OF MODIFIED CUK CONVERTER

The proposed drive is designed for a power of 400 W for household applications. The design of circuit components for dual output converter, comprises of the design of input inductor $L_i$, intermediate capacitors ($C_1$ and $C_2$), output inductors ($L_{o1}$ and $L_{o2}$), output capacitors ($C_{dc1}$ and $C_{dc2}$) and high-pass input LC filter. The selected value for the circuit inductors and capacitors after calculation and all the related motor parameters are given in Appendices. The output voltage for modified Cuk converter is given as [12],

$$V_{dc} = \frac{D}{1-D} V_{in} \sqrt{2}$$

Such that instantaneous supply voltage is given as,

$$V_{in} = [V_{o} \sin(\omega t)] = 220\sqrt{2}\sin(314t) \ V$$

A. Input Inductor ($L_i$) Design for CCM

In CCM, the current ripple is small enough, such that ac core loss is not significant. Whereas in DCM, large flux swing and high core loss occur due to high current ripple. The input inductor $L_i$ for CCM of operation, is given as [12],

$$L_i = \frac{V_{o} D(t)}{\eta \gamma^2 f_s} = \frac{R_{in} D}{\gamma f_s} = \left( \frac{V_{o}^2}{P_i} \right) \frac{D}{\gamma f_s}$$

$$= \frac{1}{\gamma f_s} \left( \frac{V_{o}^2}{P_{max}} \right) \left( \frac{V_{dc-max} + V_{in}}{V_{dc-max}} \right)$$

An equivalent input resistance is given as $R_{in}$, input power as $P_i$ and $f_s$ is taken as 20 kHz. With $V_{dc}$ as 300 V and supply voltage dip as $V_{in}=170 \ V$, the maximum ripple through input inductor can be observed. Thus the calculation of $L_i$ is given as,

$$L_i = \frac{1}{0.4 \times 20000 \left( \frac{170^2}{400} \right) \left( \frac{300}{300+170\sqrt{2}} \right)} = 5.01mH = 5mH$$

Here, an inductor current ripple ($\eta$) is considered as 40%, therefore, an input inductor is selected as 5mH.

B. Output Inductors ($L_{o1}$ and $L_{o2}$) Design for DCM

The selected DCM of operation, provides good line drawn power quality, therefore, output inductors for Cuk converter,
The capacitor voltages are kept in CCM as per the design. Therefore, permitted ripple voltage \( \kappa \) is allowed for capacitors, \( C_1 \) and \( C_2 \), thus its calculation is given as [15-17],

\[
C_1 = \frac{V_{dc} D}{\Delta V_{i} f_s R_t} = \frac{V_{dc} D}{\Delta V_{i} f_s R_t} \tag{5}
\]

For a rated DC link voltage, \( V_{dc} \) and input power \( P_i \) at this voltage, the value for load resistance \( R_L \) is given as, \( R_L = \frac{V_{dc}^2}{P_i} \). To derive the expression for calculating the values of capacitor, the value of equivalent load resistance \( R_L \) and \( V_{c(1,2)} = [V_{dc} + V_{m}] \) are substituted in (5) and final expression after rearranging is obtained as,

\[
C_1 = \frac{V_{dc}}{\kappa [V_{dc} + V_{m}] f_s (V_{dc}^2 / P_i)} \left( \frac{V_{dc}}{V_m + V_{dc}} \right)
\]

\[
= \frac{P_{\text{max}}}{\kappa (V_{dc}^2 + \sqrt{V_{dc}^2 + V_{m}^2})^2 f_s} \tag{6}
\]

Therefore, at maximum power and rated \( V_{dc} \) i.e. \( V_{dc} = 300 \text{ V} \) with as \( V_{\text{max}} = 220 \text{ V} \), the calculation for \( C_1 \) and \( C_2 \) is made for a ripple voltage \( \kappa \) as 10% as,

\[
C_1 = C_2 = \frac{400}{0.1 \times 20000 \times (220\sqrt{2} + 300)^2} = 535.50 \text{nF}
\]

This design ensures continuous voltage across two intermediate capacitors. Therefore, capacitors are selected as 690nF each.

D. Design of DC-Link Capacitor

The converter output appears across two mid-point capacitors \( \text{CdC1} \) and \( \text{CdC2} \), which are connected in series to generate midpoint N. The capacitor is determined to control \( V_{dc} \) with voltage ripple \( \lambda \) within 3\%. However, the change in \( V_{dc} \) is considered from 100 V to 300 V, therefore, output capacitor is computed by [13-15],

\[
L_0 = \frac{V_{dc} (1 - D)}{2I_{dc} f_s} = \frac{V_{dc} D}{2I_{dc} f_s} \tag{3}
\]

\[
L_0 = \left( \frac{V_{dc}^2}{P_i} \right) \left( \frac{V_{dc}}{2V_{m} f_s} \right) \tag{4}
\]

Therefore, two capacitors connected across DC link, are chosen as \( C_{dc1} = C_{dc2} = 1000 \mu F \).

E. Design of Input Filter \( (L_f \text{ and } C_f) \)

A passive LC filter is designed to eliminate switching harmonics. The peak values of input current and voltage, are denoted by \( i_m \) and \( v_m \) and displacement angle by \( \Theta \). The filter inductor \( L_f \) and filter capacitor \( C_f \) are calculated as [15-17],

\[
C_{\text{max}} = \frac{1}{\omega_i v_m} \tan(\Theta) = \frac{P_v \sqrt{2} / v_m}{\omega_i v_m}
\]

\[
= \frac{(400 \sqrt{2} / 220)}{314 \times 220} \tan(0.5\degree) = 229.69 \text{nF}
\]

Therefore, the value of \( C_f \) is taken as 220nF. The design of the input filter, is required to reduce the THD. A filter is a combination of inductor \( (L_f) \) and capacitor \( (C_f) \). The values of filter components, are designed and tuned at less than one tenth of the switching frequency. The high frequency switching harmonics are absorbed by this filter, thus acting as an input current shaper. Considering the effect of source inductance \( L_s \), the calculation is given as,

\[
L_f = L_{eq} + L_s \Rightarrow \frac{1}{4\pi^2 f_s^2 C_f} = L_{eq} + 0.04 \left( \frac{1}{\omega_i} \right) \left( \frac{V_{dc}^2}{P_i} \right) \tag{9}
\]

\[
L_{eq} = \frac{1}{4\pi^2 \times 2000^2 \times 220 \times 10^{-9}} - 0.04 \left( \frac{1}{314} \right) \left( \frac{220^2}{400} \right) = 4.4 \text{mH}
\]

Whereas a value of \( L_s \) is considered as 4\% of base impedance, thus \( L_f \) is selected as 4.5 mH.

VI. CONTROL ALGORITHM

The control of proposed drive consists of control of PFC converter and SRM. The control is designed to operate the converter at high switching frequency to obtain inherent PFC and output voltage control. The switching frequency, \( f_s \) is selected as 20 kHz to reduce the overall size of the system. To obtain PFC, two approaches are conventionally used i.e. voltage follower approach and current follower approach. Considering the cost and size constraints, the voltage follower approach is adopted here. As the sensor requirement is reduced in this approach, the size of inductor is also reduced while selecting this approach as the current through the inductor, is allowed to enter discontinuous conduction mode.

A. Control of Front-End PFC Converter

The fully controlled two equal output voltages of the converter, are varied up to 300 V to obtain motor speed
control up to 1500 rpm. It consists of a single voltage feedback loop control. This converter output DC voltage across one output capacitor \((V_{dc})\) is compared with the reference voltage \((v^*_{ref})\). The output of the comparator is an error voltage \((v_e)\) and this error voltage at any particular instant, is given as,

\[
v_e(k) = v_{ref}^*(k) - V_{dc1}(k)
\]

(10)

The controlled voltage signal is given as,

\[
v_{dc}(k) = v_{dc}(k-1) + k_p \{ v_e(k) - v_e(k-1) \} + k_i v_e(k)
\]

(11)

The controlled signal as shown in (11), is used to generate modulating signal to obtain controlled \(V_{dc}\). Where, the proportional gain is given as \(k_p\) and an integral gain is given as \(k_i\). The output of PI controller is finally compared with the high frequency carrier signal at a frequency of 20 kHz. Therefore, the generated PWM pulses are at fixed frequency and a variable duty to obtain control of \(V_{dc}\) and PFC at AC mains.

B. Control of SRM

The control of SRM requires phase to phase commutation of current in accordance with rotor position (\(θ\)), which is achieved using position sensors. Here, the optical encoders based sensors are used to determine the rotor position in the proposed drive. The motor control is based on switching sequence, which is given in Table I. The split DC converter is used to excite the motor phases with respect to switching sequence. In SRM, a discontinuous nature of the motor phase current, results in high torque ripples when one motor phase is excited at a time. Therefore, in the proposed SRM drive, the motor control is based on simultaneous excitation of two phases to get reduced torque ripples. Fig. 5 shows the path of current through motor phases during state I to state IV. However, phase A and phase B, are excited during state I, which is then followed by a state II during this state, phase B and phase C are excited. Similarly, the excitation is realised for state III and state IV.

VII. PERFORMANCE OF SRM DRIVE

To study the performance of proposed SRM drive, a prototype is developed of same motor and converter rating. The SRM is coupled to a DC generator (Benn make) feeding a resistive load bank. The voltage sensor is used to sense output capacitor voltage across one mid-point capacitor. The isolation to pulses, is provided by using an opto-coupler (IC 6N136), however, for sensing DC link voltage, a voltage sensor board is developed using a Hall-Effect voltage sensor (LV 25-P), with galvanic isolation between primary and secondary circuits. Pulse width modulated pulses for the midpoint converter and proposed PFC converter, are generated using DSP-DSpace-1104. Test results on a developed prototype, are discussed as follows.

A. Performance of Drive during Steady State Conditions

The SRM is operated while energising two motor phases at a time. The sequence for exciting the motor phases, is decided on the basis of rotor position information as shown in Table I. Here, optical encoders are used to achieve the rotor position. Fig. 6(a) shows test results obtained with two motor phases excited at the same instant as per the given switching sequence. The motor phase currents at any instant, are recorded and demonstrated in Fig. 6(b). The proposed converter possesses self-balancing of two output capacitor voltages without any voltage balancing. During two half cycles of the supply voltage, both the output capacitors are charged separately, thus maintaining \(V_{dc}\) as 300 V, with two output capacitors voltages as 150 V each, which is shown in Fig. 6(c). As per the proposed design, the speed control is obtained up to 1500 rpm with DC link voltage variation up to 300 V. Fig. 6(d) shows the improved power quality operation at rated speed as 1500 rpm and rated \(V_{dc}\) of 300V. The input current is in phase with supply voltage with reduced current THD. The motor performance is also evaluated at \(V_{dc}\) of 100 V as shown in Fig. 6(e), however, the motor speed is recorded as 490 rpm at this voltage.

<table>
<thead>
<tr>
<th>State</th>
<th>Encoder Output</th>
<th>(P_1)</th>
<th>(P_2)</th>
<th>(G_1)</th>
<th>(G_2)</th>
<th>(G_3)</th>
<th>(G_4)</th>
</tr>
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<tbody>
<tr>
<td>State I</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>State II</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>State III</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>State IV</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

TABLE I

SWITCHING STATES BASED UPON ENCODER OUTPUT
Fig. 6. Obtained results demonstrating: (a) two motor phases excitation at any instant, (b) motor current at rated speed, (c) voltage across two output capacitors as $V_{dc1} = V_{dc2} = 150\, V$, (d) improve power quality operation with $V_{dc}$ as 300 $V$, and (e) PFC operation at $V_{dc} = 100\, V$.

Fig. 7. Obtained results showing; (a) continuous capacitor voltages and discontinuous inductor currents through two Cuk converters, (b), (c) enlarge view showing DCM of operation, (d) current through input inductor and two output inductors and (e) peak current and voltage stress across the switch.
Fig. 8. Experimental results during change in \( V_{dc} \): (a) 170 V to 250 V, (b) 230 V to 150 V, (c) input voltage, input current and motor phase current during starting, (d) current in all the four motor phases during starting and (e) motor phase current with \( V_{dc} \) as 50 V.

B. Performance of Proposed Converter

The selection of magnetic component of the proposed converter is made such that output side inductor of the Cuk converter, operates in DCM and input side inductor common to both converter in CCM. Fig. 7(a) shows the voltages across both the intermediate capacitors. Moreover, these capacitors are operating in CCM as per the design. The enlarged view of Fig. 7(a) is shown in Fig. 7(b) to demonstrate the discontinuous current through output inductors. The large freewheeling current period through both the inductors, depicts the DCM of current through output inductors. The large freewheeling current period through both the inductors, depicts the DCM of operation of proposed converter. An inductor \( L_i \) operates in CCM with permissible current ripple up to 40\%. However, Fig. 7(d) shows currents through all three inductors, whereas current in high resolution mode is also shown on the figure right corner to demonstrate the sinusoidal nature of input inductor current operating in CCM. The peak voltage across and current stress through switch, are shown in Fig. 7(e). Moreover, the peak voltage stress across switch is recorded as 620 V. The peak current stress through switch, is calculated as the summation of input inductor current and output inductor current i.e., 14 A.

C. Drive Performance during Dynamic Conditions

The proposed drive is designed for the variable speeds. Therefore, the motor performance is evaluated at different dynamic conditions during the speed change. Fig. 8(a) shows the dynamics with a sudden increase in the speed with change in \( V_{dc} \). Here DC link voltage is increased from 170 V to 250 V such that change in the motor speed is observed from 760 rpm to 1240 rpm. Due to large time scale of 500 m/s and limited record length of DSO, the enlarged view is demonstrated in the same figure. Fig. 8(b) shows the dynamics with a decrease in \( V_{dc} \) from 230 V to 150 V such that a decrease in the motor speed is observed from 1210 rpm to 730 rpm. These figures show the obtained speed control with stable operation of drive after dynamic condition. Similarly, the system dynamics during starting, are also observed and shown in Figs. 8(c)-(e). Moreover, Fig. 8(d) shows the current through motor phases during starting and currents through three motor phases with DC link voltage on one channel, are shown in Fig. 8(e). The limited motor current is observed in the test results with reduced DC link voltage. Therefore, test results have demonstrated satisfactory motor performance during different conditions.

D. PFC Operation of Proposed Converter

Power quality indices such as power factor, input current THD and distortion power factor are recorded using single phase power analyser. Figs. 9(a)-(c) show the performance at converter output and input voltage as \( V_{dc}=300 \text{V} \) and \( V_{ac}=220 \text{V} \). These test results show the reduced input current THD of 4.5\% at rated load condition. The power quality parameters are also evaluated for practical supply conditions with momentarily dip in supply voltage from 220 V to 170 V. Moreover, at reduced voltage of 171.6 V, the input current THD obtained is 5.7\%, which is shown in Figs. 9(d)-(f). Similarly, Figs. 9(g)-(i) show the obtained input current THD of 5.3\% with momentarily increase in supply voltage from 220 V to 270 V. The performance is evaluated at different motor
The performance of proposed SRM drive is investigated and compared, which is shown in Fig. 10. The uncontrolled DBR fed SRM drive, consists of bulky DC link capacitor, which draws peaky current from mains with short conduction period. Moreover, the Cuk converter based SRM drive, consists of conventional Cuk converter with single output voltage. $V_{dc1}$ and $V_{dc2}$ are obtained with voltage difference between them as 2.2 V at rated DC link voltage. Whereas in DBR fed SRM drive and conventional Cuk converter fed SRM drive, the voltage differences are 8.4 V and 8.2 V. Fig. 10(a) shows the detailed comparison at different DC link voltages varying from 60 V to 300 V. Fig. 10(b) shows the input current THD over different DC link voltages. The proposed converter has high input to output voltage transfer ratio compared to conventional Cuk converter, which is shown in Fig. 10(c).
VIII. CONCLUSIONS

Test results have validated performance of proposed SRM drive. This Cuk converter with two identical output voltages, has been designed with discontinuous output inductor current. The selected inductor, has reduced the size and cost of the magnetic components. The converter output voltage is well regulated by single voltage sensor with inherent wave-shaping of input current. The wide range of speed control has also been obtained while using only one voltage sensor at converter output. Drive performance under steady and dynamics state, is found satisfactory. The input current THD of reduced value, is obtained while using only one voltage sensor at converter output. The Bode plots are shown in Fig. 11, which are obtained using transfer function for PI controller is given as,

\[ G(s) = \frac{V_o}{V_i} \]

Where \( G \) denotes the transfer function of the converter, whereas transfer function for PI controller is given as,

\[ G_c(s) = \frac{k_p}{s} + \frac{k_i}{s} \]

\[ L_{i1} = 200 \mu H \] \( C_1 = 690 nF \) and \( C_{in} = 1000 \mu F \).

APPENDIX

The DCM operation requires an additional time interval as compared to CCM operation. Either inductor current or capacitor voltage, remains zero during this time interval. Here, the first interval i.e., switch on period is considered as \( D_1T \) when the inductor current starts rising and reaches peak at the end and starts decreasing with start of interval \( D_2T \) i.e., switch off period. The time interval for constant or zero inductor current is here denoted by \( D_2T \). Choosing the input inductor current as \( i_L \), voltage across intermediate capacitor as \( V_{C1} \), output inductor current as \( i_{L2} \), and voltage across output capacitor as \( V_{dc} \) as state space variables, the state space model equations are given as,

\[ \dot{X} = A_1 X + B_1 V_G \] (12)

\[ \dot{X} = A_2 X + B_2 V_G \] (13)

\[ \dot{X} = A_3 X + B_3 V_G \] (14)

\[ V_{dc} = CX \] (15)

Where \( X \) represents state vector, \( A_1, A_2 \) and \( A_3 \) are the state matrixes, \( B_1, B_2 \) and \( B_3 \) are the input matrixes. The output state matrix is represented by \( C \) matrix, therefore, the circuit equations above state matrixes can be derived as,

\[ X = \begin{bmatrix} i_{L2} \\ V_{C1} \\ i_{L1} \\ V_{dc} \end{bmatrix} \]

\[ A_1 = \begin{bmatrix} 0 & 0 & -1/C_1 & 0 \\ 0 & 1/L_{o1} & 0 & -1/L_{o1} \\ 0 & 0 & 1/C_{dc1} & -1/C_{dc1} \end{bmatrix} \]

\[ B_1 = \begin{bmatrix} 1/L_{e1} \\ 0 \\ 0 \end{bmatrix} \]

\[ A_2 = \begin{bmatrix} 0 & -1/L_{e1} & 0 & 0 \\ 0 & 1/C_1 & 0 & 0 \\ 0 & 0 & 0 & -1/L_{o1} \\ 0 & 0 & 1/C_{dc1} & -1/C_{dc1} \end{bmatrix} \]

\[ B_2 = \begin{bmatrix} 1/L_{e1} \\ 0 \\ 0 \end{bmatrix} \]

\[ A_3 = \begin{bmatrix} 0 & -1/L_{e1} & 0 & 1/L_e \\ 0 & 0 & 1/C_2 & 0 \\ 0 & 1/L_e & 0 & -1/L_e \\ 0 & 0 & -1/C_1 & 1/L_{e1} \end{bmatrix} \]

\[ B_3 = \begin{bmatrix} 1/L_{e1} \\ 0 \\ -1/L_e \end{bmatrix} \]

Whereas, \( A = A_1D_1 + A_2D_2 + A_3D_3 \)

and, \( L_{e1} = L_e + L_{o1} \)

The interval of constant or zero inductor current can be given as, \( D_3 = 1 - (D_1 + D_2) \).

\[ G = \frac{V}{V_i} (s) = E [sI - A]^{-1} B \] (22)

Fig. 11. Bode plot of open loop and closed loop transfer function showing system stability.
Motor rating and controller gains:

\[ P_{\text{rated}} = 400W; \text{Rated speed} = 1500rpm; V_{d}(V_{dc1} + V_{dc2}) = 300V; \]

8 Stator Poles; 6 Rotor Poles; Motor phase = 4; rated torque 2.54 Nm; Motor Winding resistance \((R) = 0.7\Omega; \text{Minimum Inductance} (L_m) = 12mH; \text{aligned inductance} (L_a) = 110mH; K_p = 0.01; K_i = 0.0008.

REFERENCES


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