High-Accuracy Modelling of ZVS Energy Loss in Advanced Power Transistors

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***Abstract*— Two simulation approaches for prediction of energy loss in high-voltage power transistors (~600V) operating under ZVS (Zero-Voltage-Switching) and near-ZVS conditions are presented and proved by experiment in this work. The first approach is based on finite-element simulation whereas the second one proposes a new SPICE model. Different from prior works, both models feature Coss hysteresis and related energy loss, thus showing high precision in replicating waveforms and energy loss for real tests in the primary-side of LLC resonant converters.**

I. INTRODUCTION

The quantification of switching energy loss (E_{SW}) for high-voltage power transistors (~600V) operating under Zero Voltage Switching (ZVS) in LLC resonant converters has drastically changed during the last decade. Despite some initial works neglected E_{SW} [1,2], more up-to-date investigations point out to an increasing E_{SW} predominance in modern soft-switching converters [3,4]. From a modelling perspective, many efforts have been done to include non-linear capacitance effects [5,6] and non-ZVS operation [7] in SPICE models. However, none of these models include the most recent discoveries in output capacitance (C_{OSS}) hysteresis for Silicon SuperJunction (SJ) MOSFETs [8-11].

The energy loss related to C_{OSS} hysteresis (E_i) remains a second-order effect under hard-switching conditions [12]. Notwithstanding, it becomes crucial when operating under soft-switching conditions, especially in medium and light loads. A physical relationship between unexpected ZVS power loss and anomalous C_{OSS} hysteresis was first established in [13] for SJ MOSFETs. The experimental observations published in [8] were qualitatively reproduced in [13], elucidating the existence of E_i during C_{OSS} charge and discharge. As illustrated in Fig. 1, E_i is inherent to the SJ MOSFET architecture where, for small V_{DS}, C_{OSS} is perpendicular to the Source and Drain electrodes. Subsequently, the flow of electrons (e^-) and holes (h^+), parallel to the capacitance, sometimes originates stranded charges between the vertical N and P pillars that must be removed through a highly resistive path (depleted P and N regions).

The degree of severity varies from device to device in function of geometrical and technological features. Furthermore, no information on this effect is provided in datasheets, application notes and SPICE models. In fact, C_{OSS} provided by device vendors is typically extracted by small-signal techniques when only large-signal analysis captures C_{OSS} hysteresis. In this sense, recent works underline the need for new Figures-of-Merit and characterization techniques considering E_i [10, 14-17]. Nonetheless, available SPICE models do not yet include E_i and substantial E_{SW} inaccuracies are encountered in system efficiency predictions.

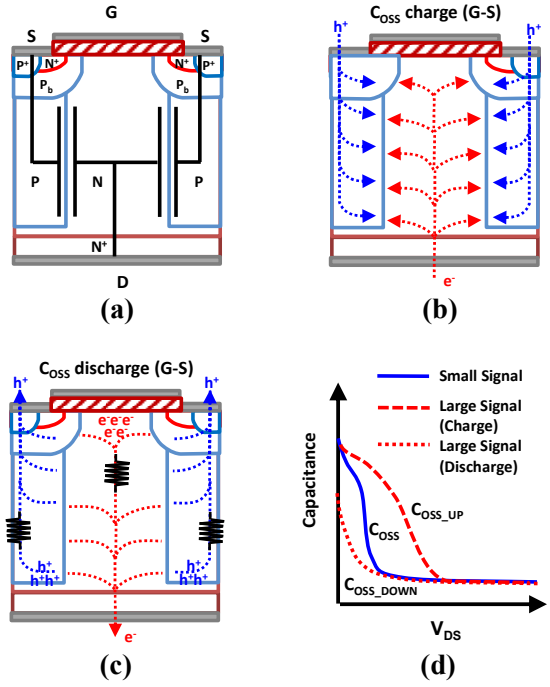


Fig. 1. (a) Cross section of a SJ MOSFET basic cell. Schematic description of (b) C_{OSS} charge and (c) C_{OSS} discharge. Electron (e^-) and hole (h^+) currents and charge pockets are indicated (red and blue). (d) Illustrative comparison between C_{OSS} extracted by small signal (solid line) and large signal (dashed and dotted lines).

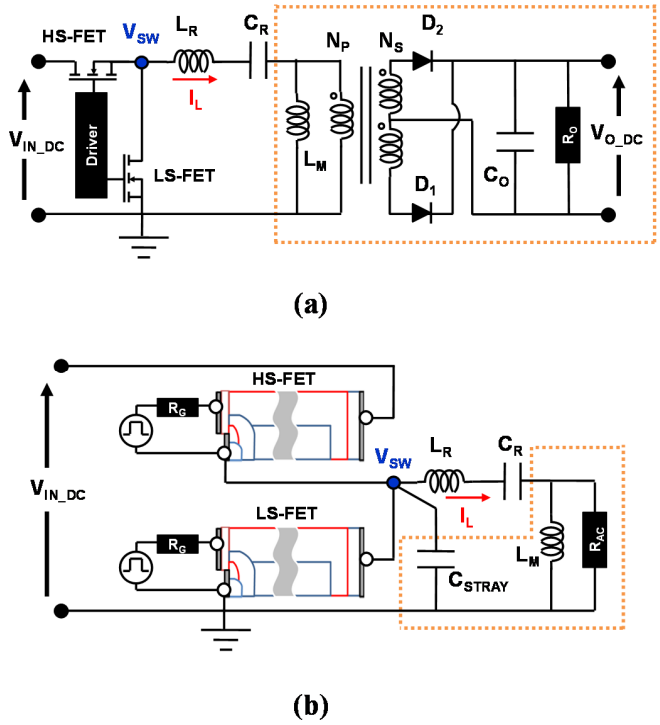


Fig. 2. (a) Schematic of half-bridge LLC resonant converter with primary and secondary sides. (b) Simplified scheme in MM simulations with focus on primary side and SJ MOSFET TCAD models.

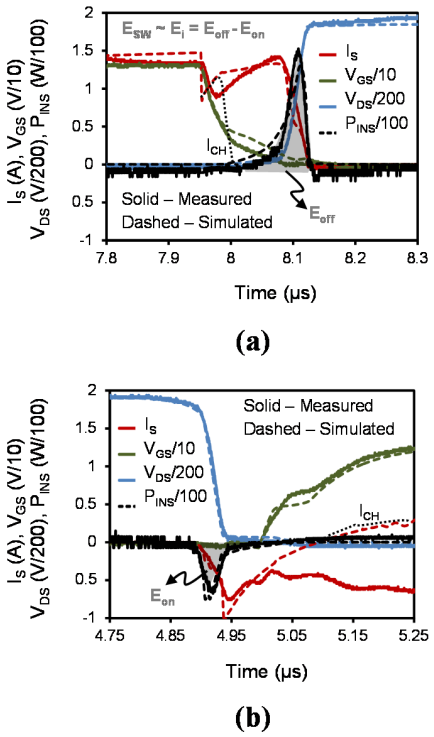


Fig. 3. Simulated and measured waveforms for LS-FET during (a) turn-off and (b) turn-on ($P_{INS} = I_S \times V_{DS}$). The I_S current contributed by the channel (I_{CH}) is represented by dotted lines.

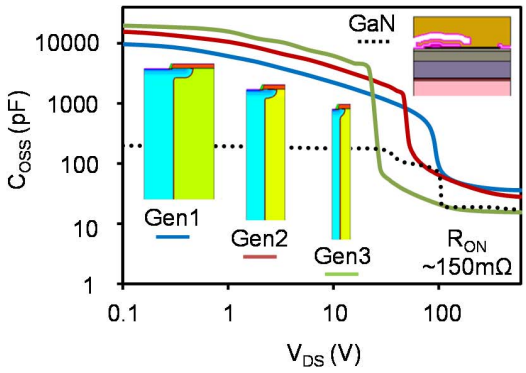
In order to improve the accuracy of power loss calculation, this work proposes and validates two different models for an existing LLC resonant converter. Firstly, Section II focuses on a high-precision model implemented by means Technology Computer-Aided Design (TCAD) physics-based simulations. Moreover, Section II analyzes E_{SW} in ZVS and non-ZVS conditions for three SJ MOSFET generations and GaN transistors. Afterwards, Section III proposes, for the first time, a SPICE-based model accounting for E_i and C_{OSS} hysteresis.

II. Mixed-Mode Simulations: Physics-Based Model

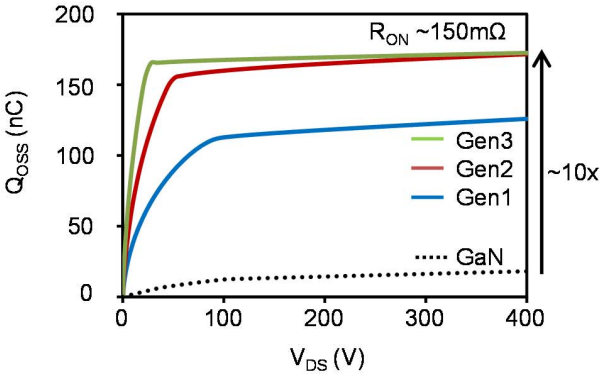
In the context of this work, Mixed-Mode (MM) simulation refers to the combined use of a SPICE circuit replacing some of their elements by finite-element structures (otherwise called TCAD structures). Hence, commercial simulation software [18] consistently solves circuit and physical equations (Poisson, e^- and h^+ current continuity) by iterative methods, matching boundary conditions in structure electrodes with circuit nodes. As shown in Fig. 2, two power switches in the primary side of a Half-Bridge (HB) LLC resonant converter have been modeled by TCAD structures. For the sake of simplicity, the secondary side and the transformer (limited by dotted lines) are replaced by equivalent R_{AC}, L_M and C_{STRAY}. Since, MM simulations require large computational time, they are normally limited to a few cycles of operation. For this reason a dynamic simulation in continuous operation normally starts from a given stationary point.

A. Experimental Calibration

The calibration process of MM simulations is done through a reference system constituted by own SJ MOSFET samples and a commercial evaluation board. On the one hand, the TCAD structure corresponding to a given SJ MOSFET (property of ON Semiconductor) has been generated by process simulation. Therefore, details in doping profiles for P and N pillars are within the TCAD model to perfectly match C_{RSS}, C_{OSS} and C_{ISS} parasitic capacitances. On the other hand, a fully documented evaluation board with a HB LLC resonant converter has been selected due to its versatility and current sensing capabilities [19]. The main characteristics of the LLC converter are a maximum output power of 600W (V_{IN_DC} = 400V, V_{O_DC} = 12V), a resonant frequency (f_{res}) of 157 kHz and an analog control with a fixed deadtime of 300 ns (t_D). The resonant tank is designed with C_R, L_R and L_M of 66nF, 15.5uH and 195uH, respectively. The SJ MOSFET electrical requirements related to resonant tank and t_D are fulfilled to ensure ZVS inductive mode in the entire load range. An initial R_{AC} is guessed by First Harmonic Approximation (FHA) theory. Afterwards, the theoretical R_{AC} needs a refinement to match the measured waveforms. Another relevant fitting parameter accounting for the transformer parasitic capacitance is C_{STRAY}. A proper calibration of C_{STRAY} is achieved by the measured slope of the switching node voltage (V_{SW}). A correction on the simulated frequency needs to be introduced to counteract the I_L distortion originated by the secondary side before switching.



(a)

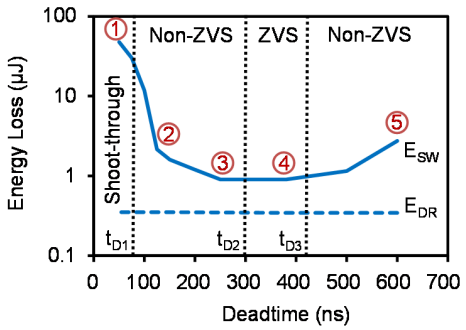


(b)

Fig. 4. (a) C_{OSS} vs. V_{DS} extracted by small signal analysis with MM simulations for three different SJ MOSFET generations and E-Mode GaN (all of them scaled to R_{ON} ~ 150mΩ). TCAD structures for all devices are included. (b) Q_{OSS} vs. V_{DS} derived from C_{OSS} in (a).

The accuracy of this calibration is exhibited in Figs. 3a and 3b for turn-on and turn-off transients. The match between simulation (dashed lines) and experiment (solid lines) shows a less than 15% error in E_{SW}. Even more, some details of the waveforms that were never reproduced by SPICE models are now present. An example is the V_{SW} ramp asymmetry (corner sharpness at bottom and top in Fig. 3a and 3b), thus pinpointing an uneven charge and discharge of C_{OSS} in both HS-FET and LS-FET. In the following sections, $V_{DS\_LS} \sim V_{SW}$ and $V_{DS\_HS} \sim V_{IN\_DC} - V_{SW}$ are usual approximations.

A physical inspection of e^- and h^+ currents reveals that the I_S contribution of the channel current (I_{CH}) is negligible during C_{OSS} charge/discharge. This fact confirms that C_{OSS} discharge through the channel does not occur when turning-off the power transistor, thus obeying to a Zero Current Switching (ZCS) scenario. Note that $I_{CH} \sim 0$ cannot be inferred from current sensed at drain or source. As a result of the combined ZCS turn-off and ZVS turn-on, E_{SW} is purely related to the C_{OSS} charge/discharge ($E_{SW} \sim E_i$). In the next section, other scenarios are presented where Non-ZVS will determine $E_{SW} > E_i$.



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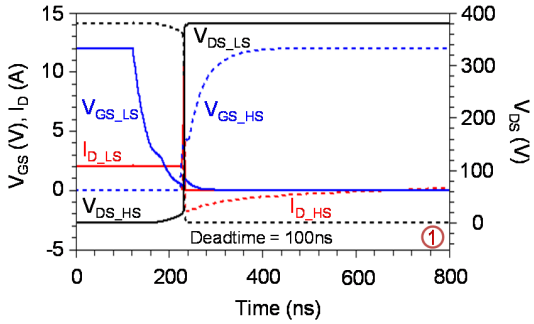

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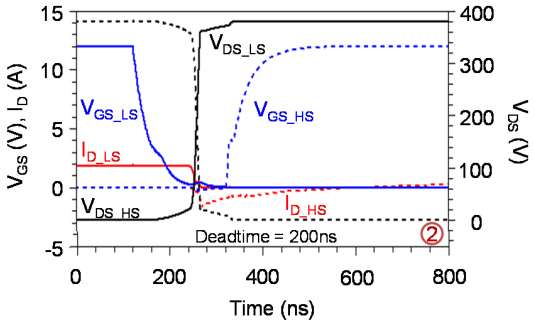


(c)

Fig. 5. (a) MM simulation analysis of driving and switching energies (E_{SW} and E_{DR}) vs. deadtime (t_D) for SJ MOSFET Gen3. (b),(c) V_{GS}, V_{DS} and I_D waveforms for LS and HS-FETs in regimes (1),(2) indicated in Fig. 5a.

B. Analysis of ZVS and Non-ZVS Operation

A more generic SJ MOSFET TCAD structure is evaluated by using calibrated MM simulations. This structure is parametrized in terms of P and N pillar width and doping concentration. Three substructures labelled as Gen1, 2 and 3 (Fig. 4a) are generated by varying the pillar widths with constant total charge density (~ 1×10^{12} cm^{-2}) and their area is scaled to 150 mΩ on-state resistance (R_{ON}). The goal is to emulate three generations that are representative of the SJ MOSFET evolution during the last 15 years. The R_{ON} per unit area is 35, 24 and 10 mΩ×mm^2 for Gen1, 2 and 3, respectively.

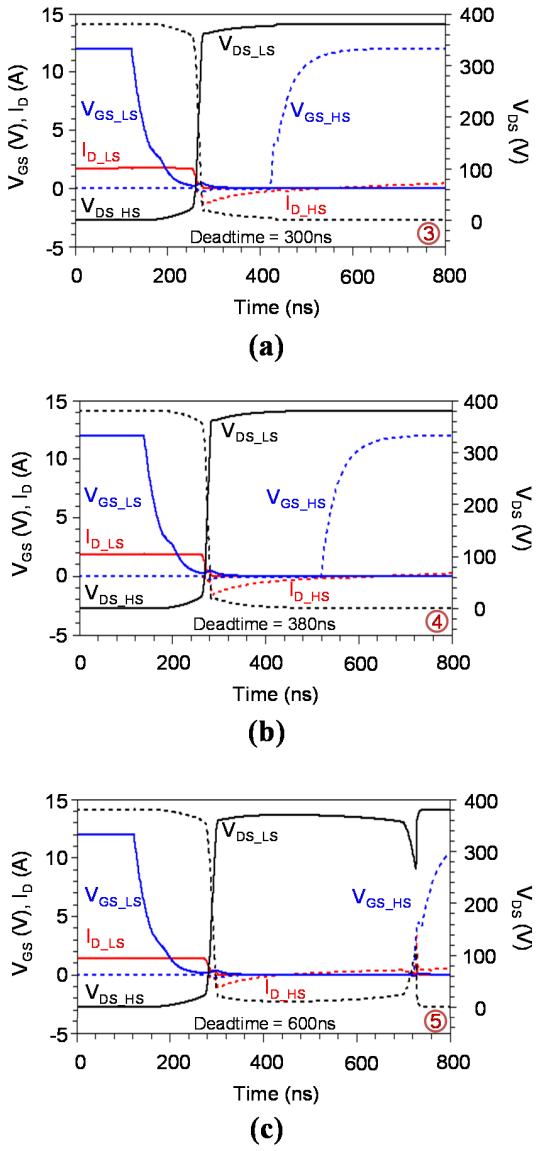


Fig. 6. (a),(b),(c) V_{GS}, V_{DS} and I_D waveforms for LS and HS-FETs in regimes (3),(4),(5) indicated in Fig. 5a.

Among other electrical parameters, the three substructures correctly reproduce the transformation of C_{OSS} and Q_{OSS} vs. V_{DS} with the maturation of the SJ MOSFET technologies [20]. As shown in Fig. 4a and 4b, the newest generations sharply increase Q_{OSS} with a relatively small V_{DS}. This is a direct consequence of the more abrupt PN vertical junction for small pitch and high-density current transistors.

In order to investigate the impact of ZVS and Non-ZVS on different energy losses, SJ MOSFET Gen3 has been simulated for different t_D and operating frequency (f_{SW}) below the resonant one ($f_{res} > f_{SW} >> 1/t_D$). A U-shape dependence of E_{SW} vs t_D is evidenced in Fig. 5a with five different regimes:

(1) $t_D < t_{D1}$ where $t_{D1} = 2\times Q_{GS}/I_G$ and cross conduction produces large E_{SW} ($E_{SW} >> E_i$).

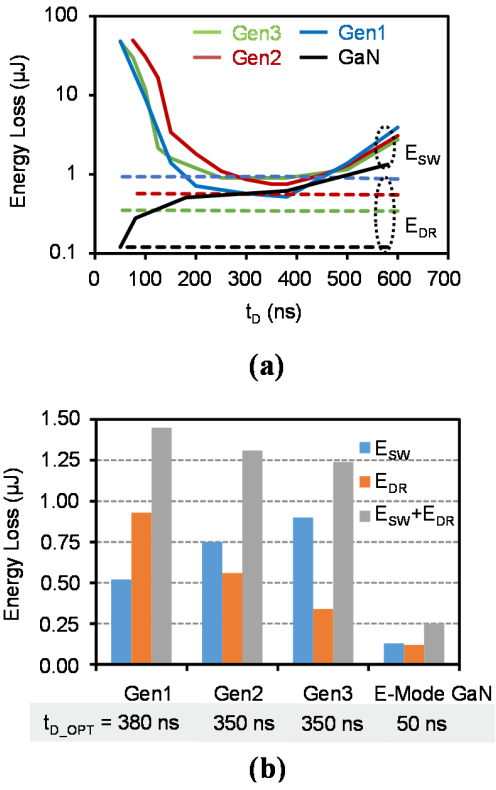


Fig. 7. (a) E_{SW} & E_{DR} vs. deadtime (t_D) calculated by MM simulations with LLC circuit scheme in Fig. 1 and device structures in Fig. 3a. (b) E_{SW} & E_{DR} contributions at optimum t_D (t_{D_OPT}) in each transistor. E_{SW} includes parasitic diode loss (E_{DIO}), negligible for SJ-FETs but noticeable for E-Mode GaN.

(2) & (3) $t_{D1} < t_D < t_{D2}$ where $t_{D2} = 16\times f_R\times L_M\times Q_{MAG}/V_{DD}$ and Q_{MAG} is the magnetizing current charge. Despite both (2) & (3) are Non-ZVS with incomplete discharge of parasitic capacitances, the non-linear C_{OSS} vs. V_{DS} produces substantial E_{SW} variation between (2) & (3) ($E_{SW} = E_i + E_{NON\text{-}ZVS}$).

(4) $t_{D2} < t_D < t_{D3}$ where $t_{D3} = t_{D2} + \theta/\omega R$ where θ and ωR are a load angle and LC angular frequency described in [21]. In this regime a perfect ZVS is achieved with $E_{SW} = E_i$.

(5) $t_{D3} < t_D$. When t_D is too large a recharge effect of C_{OSS} occurs with subsequent Non-ZVS and additional energy loss ($E_{SW} = E_i + E_{NON\text{-}ZVS}$).

V_{GS}, V_{DS} and I_D waveforms corresponding to each one of these five regimes are provided in Figs. 5 and 6 for LS and HS-FETs. For very short t_D, the crossing between V_{GS} waveforms (Fig. 5a) evidences the shoot-through predominance in regime (1). A sudden V_{DS} rise/fall in LS/HS and the existence of V_{GS} Miller plateau are Non-ZVS indicators (Figs. 5c and 6a). However, Non-ZVS in SJ MOSFETs is likely to occur in the high C_{OSS} region, where V_{DS} is relatively low (< 50V). As a result, in spite of showing Non-ZVS, regime (3) has identical E_{SW} compared regime (4) with ZVS (Fig. 6b). For very large t_D, the partial V_{DS} rise/fall in HS/LS (Fig. 6c) shows that C_{OSS} starts being discharged/charged in LS/HS. It is worth to remark that, differently from E_{SW}, the driving energy loss (E_{DR}) is practically independent of t_D (less than 15% shift) [7].

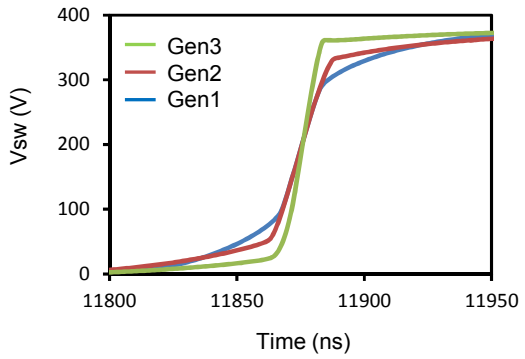


Fig. 8. Simulated V_{SW} vs. time during LS-FET turn-off in SJ MOSFET Gen1, 2 and 3. The assimetry between top and bottom corners is more pronounced in Gen3.

C. *Prospective Analysis in Si and GaN power transistors*

The analysis in Subsection II.B for SJ MOSFETs Gen3 is now extended to Gen1 and 2. Regarding the dependency of E_{SW} with t_D, common trends at short and large t_D are observed from Fig. 7a. In spite of this, Gen 1 and 2 show a more gradual increase of Non-ZVS loss in agreement with a smother C_{OSS} vs. V_{DS} non-linearity. Fig. 7b displays the energy loss contributions for the optimum t_D in Fig. 7a (t_{D_OPT}). As long as SJ MOSFETs evolve to newer generations, E_{DR} and E_{SW} show opposite trends: E_{DR} decreases and E_{SW} increases. As a matter of fact, a substantial gate charge reduction (Q_G) causes an E_{DR} drop whereas E_i is boosted by narrower P and N pillars. The signature of C_{OSS} hysteresis is manifested in Fig. 8 by V_{SW} waveforms. Indeed, Gen3 shows a corner of almost 90° at the top in contrast with a smother corner at the bottom. For Gen1 and 2 the corners feature higher symmetry. Hence, the total energy losses are eventually reduced in advanced Gen3, however, E_i remains a major obstacle for further improvement. In this scenario, GaN transistors are promising candidates for the next evolutionary step. Not only to break the well-known Q_{OSS} and Q_{GS} Silicon limits but to mitigate E_i as well. More specifically, E-Mode GaN transistors enable a breakthrough of 10x reduction in Q_{OSS} and Q_{GS} with respect to SJ MOSFET Gen3 when scaling to the same R_{ON} = 150 mΩ. A possible optimization in the resonant tank for lower Q_{OSS} is not contemplated in this work. The E_{SW} benefits when using E-Mode GaN are not observed for t_D > 250 ns due to the relevance of the third quadrant loss (parasitic diode loss E_{DIO}). It is noteworthy that SJ MOSFETs and GaN transistors are driven between [+12V,0V] and [+6V,-3V], respectively. Differently, E_{SW} is drastically reduced for t_D < 250 ns in GaN with a 5x total energy loss at t_D = 50 ns (Fig. 7b). This achievement is partially due to the residual E_i in E-Mode GaN transistors that becomes only noticeable when charging and discharging C_{OSS} at very-high-frequency (> 10MHz) [16].

III. SPICE Simulations: Behavioral Model

Using the scheme proposed in Fig. 2b and replacing the SJ MOSFETs TCAD models by SPICE models, a simulation is carried out. In this simulation, the proposed SJ MOSFETs SPICE models are developed using different values of output capacitance when it is charged or discharged. The model includes both C_{OSS} non-linearity and hysteresis. C_{OSS_UP} (V_{DS}) and C_{OSS_DOWN} (V_{DS}), described in Fig. 1d, are used when the output capacitance is charged (turn-off of the MOSFET) and discharged (turn-on of the MOSFET), respectively. When V_{SW} ramps up (i.e. turn-off of LS-FET and turn-on of HS-FET) C_{OSS_UP} (V_{DS}) is applied to LS-FET and C_{OSS_DOWN} (V_{DS}) is applied to HS-FET. Conversely, when V_{SW} ramps down (i.e. turn-on of LS-FET and turn-off of HS-FET) C_{OSS_DOWN} (V_{DS}) is applied to LS-FET and C_{OSS_UP} (V_{DS}) is applied to HS-FET.

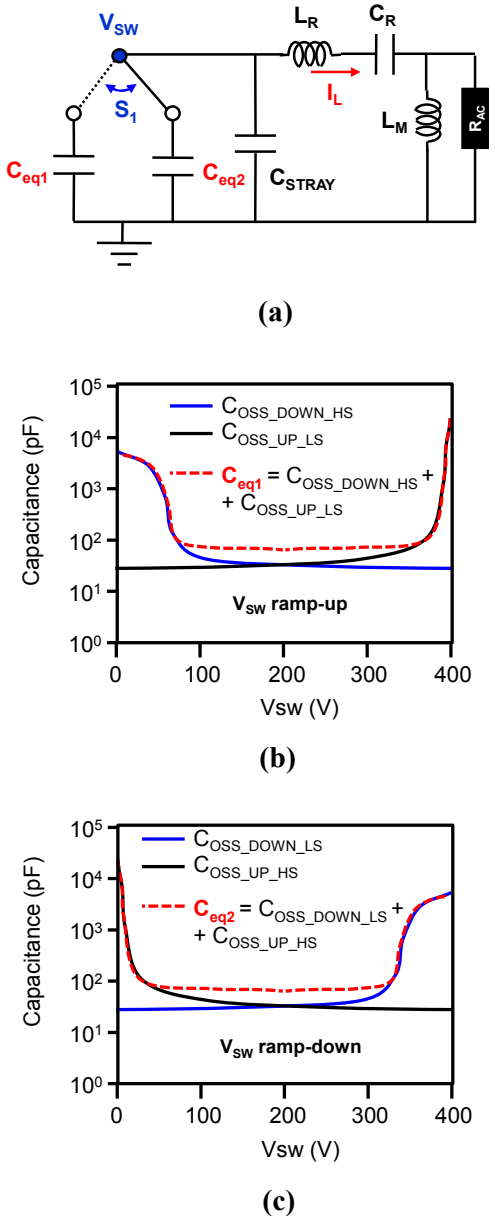
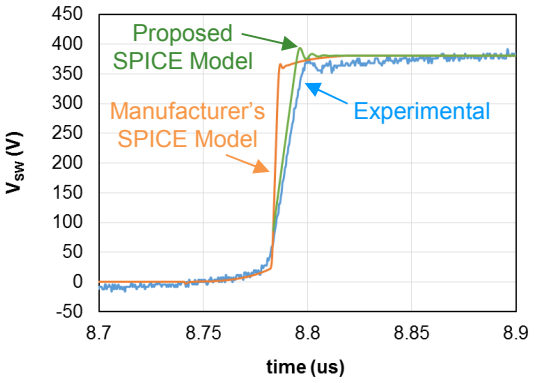


Fig. 9. (a) Equivalent LLC circuit with dual capacitor SPICE model to account for E_i and C_{OSS} hysteresis. Equivalent capacitances $C_{eq1,2}$ vs. V_{SW} for (b) V_{SW} ramp up and (c) V_{SW} ramp down. $C_{eq1,2}$ are asymmetric with respect to charge/ discharge of LS-FET and HS-FET.



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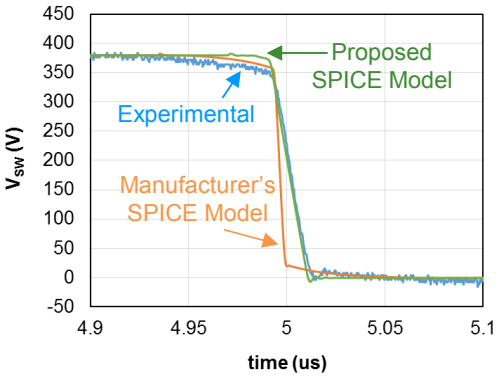

(b)

Fig. 10. V_{SW} vs. time extracted by measurement (blue), manufacturer's SPICE model (orange) and proposed SPICE model (green) during (a) V_{SW} ramp up and (b) V_{SW} ramp down.

Hence, $C_{eq1,2}$ are derived from these capacitive combinations during V_{SW} ramp up and down, respectively, as schematically represented in Figs. 9b and 9c. A similar strategy, named "dual capacitor model", has been used in previous literature to create SPICE models for ferroelectric capacitors [22]. Since $C_{eq1,2}$ are asymmetric, an energy E_i is associated to V_{SW} ramp up and down for every cycle of the system. This energy is merely calculated from:

$$E_i = E_{ramp\_up} - E_{ramp\_down} \quad (1)$$

being:

$$E_{ramp\_up} = \int_0^{V_{IN\_DC}} C_{eq1}(V_{SW}) \cdot V_{SW} \cdot dV \quad (2)$$

$$E_{ramp\_down} = \int_{V_{IN\_DC}}^{0} C_{eq2}(V_{SW}) \cdot V_{SW} \cdot dV \quad (3)$$

Fig. 10 compares measured V_{SW} waveform, manufacturer's SPICE model and proposed SPICE model. The new model captures the corner asymmetry when V_{SW} ramps up and down during LS-FET turn-off and turn-on transitions, thus being consistent with the E_i existence and also having an influence in the quantification of Non-ZVS energy loss.

IV. Conclusions

Switching losses in high-voltage power switches during ZVS operation mode are assessed in this work by means of two different modelling strategies based on finite-element and SPICE simulations. In both cases, C_{OSS} hysteresis and intrinsic energy loss are included and their relevance is validated by means of measurements in an LLC resonant converter. After studying by simulation three SJ MOSFET generations, it is inferred that, adding to the well-known Q_{OSS} and Q_{GS} limitations, E_i becomes crucial and new modelling strategies urge in advanced Si technologies.

Acknowledgment

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References

[1] C. E. Person, "Selection of primary side devices for LLC resonant converters". Doctoral dissertation, Virginia Tech, 2008.

[2] R. Yu, G. K. Y. Ho, B. M. H. Pong, B. W. K. Ling, and J. Lam, "Computer-aided design and optimization of high-efficiency LLC series resonant converter," IEEE Transactions on Power Electronics, 27(7), pp. 3243-3256, 2012.

[3] K. Tabira, S. Watanabe, T. Shimatou, and T. Watashima, "Advantage of super junction MOSFET for power supply application," in 2014 IEEE Power Electronics Conference (ECCE-ASIA), pp. 2939-2943, 2014.

[4] W. Zhang, F. Wang, D. J. Costinett, L. M. Tolbert, and B. J. Blalock, "Investigation of gallium nitride devices in high-frequency LLC resonant converters," IEEE Transactions on Power Electronics, 32(1), pp. 571-583, 2017.

[5] R. Elferich, "General ZVS half bridge model regarding nonlinear capacitances and application to LLC design," in 2012 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 4404-4410, 2012.

[6] D. Costinett, D. Maksimovic, and R. Zane, "Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies," IEEE Transactions on Power Electronics, 30(2), pp. 985-995, 2015.

[7] C. Oeder, M. Barwig, and T. Duerbaum, "Estimation of switching losses in resonant converters based on datasheet information," in IEEE European Conference on Power Electronics and Applications (EPE-ECCE Europe), pp. 1-9, 2016.

[8] J. B. Fedison, M. Fornage, M. J. Harrison, and D. R. Zimmanck, "Coss related energy loss in power MOSFETs used in zero-voltage-switched applications," in 2014 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 150-156, 2014.

[9] R. Miftakhutdinov, "New ZVS analysis of PWM converters applied to super-junction, GaN and SiC power FETs," in 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 336-341, 2015.

[10] X. Li and A. Bhalla, "Comparison of intrinsic energy losses in unipolar power switches," in 2016 IEEE Wide Bandgap Power Devices and Applications (WiPDA), pp. 228-232, 2016.

[11] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," IEEE Transactions on Power Electronics, 31(12), pp. 8063-8067, 2016.

[12] I. Castro, J. Roig, R. Gelagaev, B. Vlachakis, F. Bauwens, D. G. Lamar, and J. Driesen, "Analytical switching loss model for superjunction MOSFET with capacitive nonlinearities and

displacement currents for DC–DC power converters," IEEE Transactions on Power Electronics, 31(3), pp. 2485-2495, 2016.

[13] J. Roig and F. Bauwens, "Origin of Anomalous Coss Hysteresis in Resonant Converters With Superjunction FETs," IEEE Transactions on Electron Devices, 62(9), pp. 3092-3094, 2015

[14] J. B. Fedison and M. J. Harrison, "COSS hysteresis in advanced superjunction MOSFETs," in 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 247-252, 2016.

[15] R. Miftakhutdinov, "Analysis and Practical Method of Determining WBG FET Switching Losses Associated with Nonlinear Coss," in 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 974-978, 2017.

[16] S. Park and J. M. Rivas, "Power Loss of GaN Transistor Reverse Diodes in a High Frequency High Voltage Resonant Rectifier," in 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 1942-1945, 2017.

[17] D. Neumayr, M. Guacci, D. Bortis, and J. W. Kolar, "New calorimetrie power transistor soft-switching loss measurement based on accurate temperature rise monitoring," in 2017 IEEE International Symposium on Power Semiconductor Devices and IC's (ISPSD), pp. 447-450, 2017.

[18] Sentaurus TCAD Tools Suite. Synopsys 2016.

[19] A. Steiner, F. Di Domenico, J. Catly, F. Stückler, "600W half bridge LLC Evaluation Board with 600V CoolMOS™ C7", Infineon Technology AN – June 2015.

[20] M. Treu et al., "The role of silicon, silicon carbide and gallium nitride in power electronics," in 2012 IEEE International Electron Devices Meeting (IEDM), pp. 7-11, 2012.

[21] R. Ren et al. "Accurate ZVS Boundary in High Switching Frequency LLC Converter, " in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1-6, 2016.

[22] A. Sheikholeslami and P. G. Gulak, "A survey of behavioral modeling of ferroelectric capacitors," IEEE transactions on ultrasonics, ferroelectrics, and frequency control, 44(4), pp. 917-924, 1997.