Generalized SVPWM-based Capacitor Voltage Balancing for Modular Multilevel Converters

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***Abstract*—Submodule (SM) capacitor voltage and arm voltage balancing are imperative for the reliable operation of modular multilevel converters (MMCs). In this paper, a new, simple and generalized discontinuous space-vector pulse width modulation (PWM)-based SM capacitor voltage balancing approach is proposed and developed within the carrier-based PWM for MMCs. Discontinuous modulation can be achieved by addition of zero-sequence component to the PWM modulator so that MMC arm is clamped to positive or negative dc-bus during a particular interval. In addition, a simple generalized approach for determination of zero-sequence component using the zero vector distribution factor is proposed. The dynamic performance of the proposed generalized discontinuous modulation technique and voltage balancing approach for half-bridge (HB)-SM based 5-level MMC is demonstrated through simulation results in PLECS platform. The proposed scheme is applicable to any number of SMs, any SM type and balanced or unbalanced phase voltages.**

***Index Terms*—Modular multilevel converters, motor drives, power electronics, rail transportation, road transportation, space vector pulse width modulation, total harmonic distortion.**

I. Introduction

Over the past years, the commerical products have been developed using modular multilevel converters (MMCs) in the field of high-voltage direct current (HVDC) transmission [1], [2], high-power medium voltage motor drives [3], medium-voltage static compensator (STATCOM) [4] and battery energy storage sytems [5]. Recently, MMCs have emerged as a promising converter topology for electric transportation applications such as battery charging infrastructure [6], and propulsion systems for electric railway traction [7], emerging electric ship [8], and battery electric vehicles [6], [9]. These converters offer some salient features such as modularity, scalability to higher power and voltage levels, low harmonic contents, high efficiency, high availability, inherent redundancy, lower electro-magnetic interface and no bulk dc-link capacitors [10].

SM capacitor voltage balancing, the arm/leg voltage balancing and circulating current suppression controllers are critical for the safe and reliable operation of MMC. The different closed loop capacitor balancing controllers with phase-shifted or phase-disposition PWM (PS-PWM, PD-PWM) scheme used to achieve SM capacitor voltage balancing are addressed in [10]–[12]. However, these approaches require balancing and averaging proportional-integral (PI) controllers and also the design of the multiple PI controllers are quite difficult. SM capacitor voltage balancing can be performed at the modulation stage based on sorting algorithms and the arm current direction to make a decision to activate or bypass SMs [2], [13]. A circulating current suppression control with a zero-sequence voltage injection is incorporated with the modulation scheme such as nearest level control (NLC) [14], carrier-based PWM [15] and model predictive control methods [16].

The arm balancing without any closed loop controller can be achieved by space-vector PWM (SVPWM) as it has more freedom to choose the voltage vectors with different zero sequence voltage magnitudes [13]. These modulation strategies can be classified based on zero-vector placement as continuous and discontinuous PWM (CPWM, DPWM). Compared to the CPWM, DPWM reduces the inverter switching losses and improved harmonic characteristics at higher modulation indices in two-level and multi-level converters [17]. A preliminary study of DPWM on MMC based on clamping arm to a non-switching position is addressed in [18]. This clamping effect is achieved through a closed-loop control of circulating current and addition of a zero-sequence component. The DPWM is able to reduce the switching losses as well as SM capacitor voltage ripples especially at low modulation indices which is desirable feature for motor drive applications. However, this method requires additional SMs in each arm for control and also has no freedom to choose between different zero-sequence voltage vectors. A new approach of DPWM without additional SMs is presented in [19], the arm with the highest or lowest modulation signal is clamped irrespective of upper or lower arm which is called “virtual clamping”. This method helps to avoid additional SMs which implies a reduction in conduction losses and converter costs. However, switching losses and the capacitor voltage ripples are less significant compared to DPWM in [18].

This paper presents a new generalized discontinuous SVPWM-based capacitor voltage balancing approach for MMC with significant features: (i) a simple and easy implementation with any type of discontinuous PWM techniques (ii) utilizes a generalized approach to determine the various zero-sequence components (iii) easily extended to any number of SMs and any SM type (iv) the redundant switching state selection is simple (v) this approach regulates all capacitor voltages within a nominal value without any balancing PI-controller. The proposed method is very simple, computational efficient and easily implemented in DSP and/or FPGA. The steady-

state and dynamic performances of proposed SVPWM-based voltage balancing approach is verified on a 5-level MMC (4 SMs per arm) with two-level HB-SMs. The key performance indices such as waveform quality, dc-bus current ripple and SM capacitor voltage ripple for different DPWM techniques are holistically evaluated and compared with SVPWM scheme.

II. Modeling and Control of the MMC

The MMC consists of two arms per leg, where each arm comprises of "N" identical series connected SMs through an arm inductor (L_{arm}). Fig. 1(a) shows the configuration of three-phase MMC with two-level HB-SMs [Fig. 1(b)]. The output voltage variation depends on the charging and the discharging of the capacitor voltages with the direction of the current flowing in or out of SM. The four possible switching states of HB-SM are given in Table I. The voltage difference

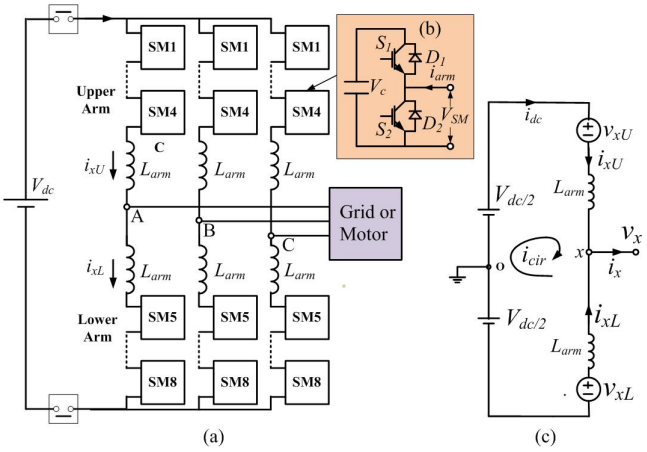

Fig. 1. The single-phase equivalent of three-phase MMC with HB-SMs.

between the upper and the lower arms will appear across the L_{arm} results in circulating currents. This can be analyzed by considering the dynamic behavior of the arm currents [16]. The arm current consists of input source current (i_{dc}), output current (i_x) [$x \in \{a, b, c\}$], and circulating current (i_{cir}). From

TABLE I
Switching States of Two Level-HBSM

$State$	S_1	S_2	i_{arm}	V_c	V_{SM}
1	1	0	>0	$v_c\uparrow$	V_c
2	1	0	<0	$v_c\downarrow$	V_c
3	0	1	>0	$v_c\approx$	0
4	0	1	<0	$v_c\approx$	0

the single-phase equivalent circuit shown in Fig. 1(c), the upper i_{xU} and lower arm currents i_{xL} can be expressed as:

$$i_{xU} = \frac{i_{dc}}{3} + i_{cir} + \frac{i_x}{2} \tag{1}$$

$$i_{xL} = \frac{i_{dc}}{3} + i_{cir} - \frac{i_x}{2} \tag{2}$$

The output and circulating currents can be calculated from above equations:

$$i_x = i_{xU} - i_{xL} \tag{3}$$

$$i_{cir} = \frac{i_{xU} + i_{xL}}{2} - \frac{i_{dc}}{3} \tag{4}$$

$$i_{cir} = \overline{i_{cir}} + \widetilde{i_{cir}} \tag{5}$$

The dc component ($\overline{i_{cir}}$) is responsible for the energy transfer in each leg, where as the ac component ($\widetilde{i_{cir}}$) originates due to voltage fluctuations in SM capacitors. These currents increase the converter power losses and the capacitor voltage ripples. The arm inductors are used to control these currents within the phase legs and to limit in-rush currents during pre-charging of the capacitors. The modulating signal can be represented by

$$V_{xo} = m \times \frac{V_{dc}}{2} \times cos(\omega t + \varphi) \tag{6}$$

where $0<m<1$ is the modulation index, φ is the initial phase

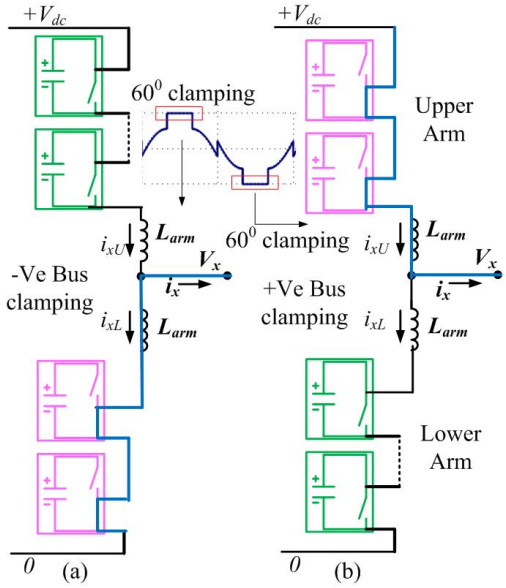

Fig. 2. Circuit operation of MMC when clamping to the (a) negative dc-bus (b) positive dc-bus (green: activated SMs and pink: bypassed SMs).

angle and ω is the supply frequency in rad/s. The normalized reference modulating signals for upper V_{xU}^{ref} and lower arm V_{xL}^{ref} is given as:

$$V_{xU}^{ref} = \frac{1}{2}[1 - m \times cos(\omega t + \varphi)] \tag{7}$$

$$V_{xL}^{ref} = \frac{1}{2}[1 + m \times cos(\omega t + \varphi)] \tag{8}$$

III. Generalized Discontinuous SVPWM-based PWM and Voltage Balancing Algorithm

A. Discontinuous Modulation

The DPWM technique consists of injecting zero-sequence signal to the original modulating signal such that one of the arm in the phase leg of MMC is clamped to positive or negative dc-bus for some intervals. Fig. 2 shows the circuit operation of MMC during positive and negative dc-bus clamping. Due to zero-sequence injection, linear mode operation of MMC is increased i.e maximum achievable modulation index m = 1.15.

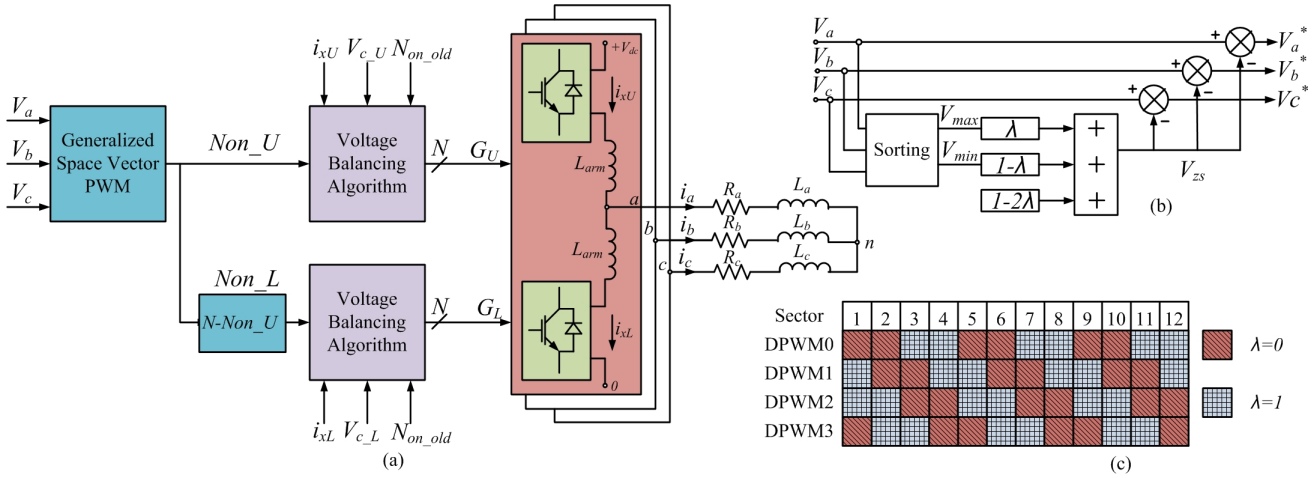

Fig. 3. (a) Block diagram of proposed generalized SVPWM and voltage balancing algorithm (b) Block diagram of carrier based zero-sequence voltage injection (c) λ determination for different discontinuous PWM techniques.

Moreover, since there is always one arm without switching during clamping interval, the switching losses of the MMC is reduced. Various DPWM techniques applied to multi-level converters [20], [21]. DPWMMAX, DPWMMIN, DPWM0, DPWM1, DPWM2 and DPWM3 are popular ones in addition to SVPWM. DPWM technique was applied to MMC [18], [19], in which all the SMs of one arm are bypassed during clamping interval and current flows through the arm is shown in Fig. 2. Moreover, another benefit achieved in MMC is a reduction in SM capacitor voltage ripple and hence in circulating currents. The detailed explanation on SM capacitor voltage reduction analysis using DPWM is found in [18].

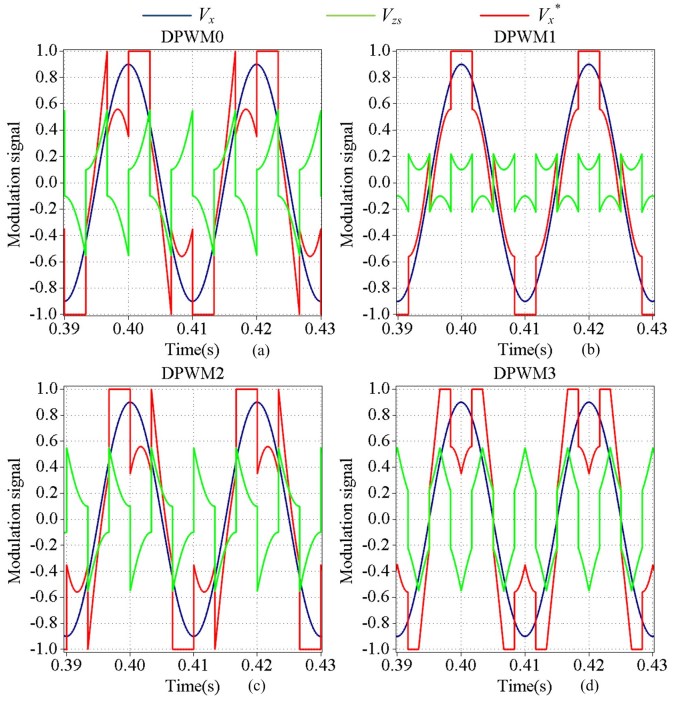

Fig. 4. Normlized modulation signal of discontinuous PWM techniques.

B. Generalized Space-vector PWM

The control block diagram of generalized discontinuous SVPWM for MMC is shown in Fig. 3(a). The normalized phase modulating signals are generated from the synchronous dq-frame current controller and the field orientated controller in case of grid connected systems and motor drives respectively. The normalized modulation signals for upper and lower arms calculated from Eq. (6) and (7) are passed to generalized SVPWM block. The zero-sequence voltage injection signal is generated based on type of DPWM technique and is added to original modulation signal (V_x), thus the modulation signal (V_x^*) is modified as:

$$V_x^* = V_x + V_{zs} \tag{9}$$

The normalized zero-sequence voltage injection signal V_{zs} is calculated by [21] :

$$V_{zs} = (\lambda - 1) \times V_{min} - \lambda \times V_{max} + (2 \times \lambda - 1) \tag{10}$$

where V_{max} and V_{min} are the instantaneous maximum and minimum magnitudes of the balanced three-phase voltages. The block diagram representation of zero-sequence voltage signal is shown in the Fig. 3(b) and their output (V_{zs}) depends on the zero vector distribution factor (λ). In this paper, the representation of multilevel SVPWM mapping to two-level space-vector PWM is discussed. The required sinusoidal output voltage over one cycle (2π) is divided into tweleve sectors and each sector covers a duration of $\pi/6$. Thus, the zero vector distribution factor (λ) is determined from twelve-sector space-vector diagram corresponding to DPWM type based on the location of the sector as shown in Fig. 3(c). This is a simple and easy approach which does not require any complex calculations.

The normalized modulation signals for 60^o clamping methods such as DPWM0, DPWM1, DPWM2 and DPWM3 is shown in Fig. 4(a)-(c). DPWM3 is one kind of split-clamping where the clamping period is split into two 30^o intervals during half-cycle (Fig. 4(d)). The range of λ is defined as ($0 \leq \lambda \leq 1$), when λ = 0.5 corresponding to conventional SVPWM.

In DPWMMAX (λ = 1) and DPWMMIN (λ = 0) schemes, each of the phase legs is clamped for 120^o, therefore these schemes do not have much significance in case of MMCs. The new normalized reference modulation signals are generated adding a zero-sequence component which is obtained by Eq. (10) to original modulation signals are shown in Fig. 4. The generated modulation signals are compared with triangular carrier signals (PS-PWM or PD-PWM) and each output is added together to generate normalized PWM (N_{on}), which is passed to voltage balancing algorithm block. The normalized PWM (N_{on}) represents the number of SMs to be activated at any given instant. To reduce the additional computations, normalized PWM for lower arm can be obtained by satisfying the following equation.

$$N = N_{xU} + N_{xL} \tag{11}$$

Finally, normalized PWM is passed to voltage balancing algorithm block which will be explained in next section.

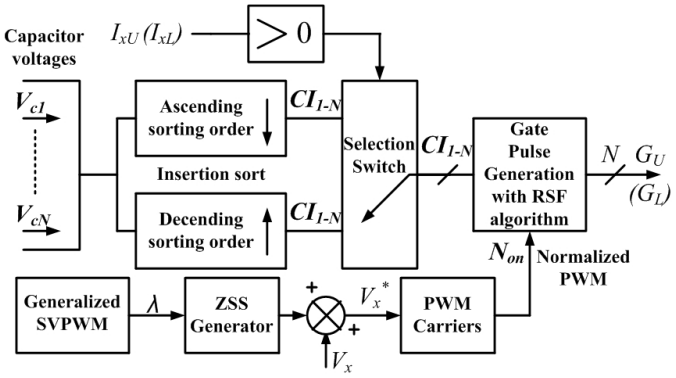

Fig. 5. Block diagram of proposed SM capacitor voltage-balancing algorithm.

C. Capacitor Voltage Balancing Approach

The principle of the SM capacitor voltage balancing algorithm is to charge and discharge capacitors based on instantaneous values of capacitors and the arm current direction. The block diagram of proposed balancing algorithm is implemented in two main stages as shown in Fig. 5.

1) Generation of SM capacitor index number: In this approach, the cells with the highest voltage are inserted to discharge the capacitors for positive arm current direction (i_{xU} (i_{xL}) $>$ 0). Similarly, the cells with the lowest voltage are inserted to charge the capacitors for negative arm current direction (i_{xU} (i_{xL}) $<$ 0). This objective can be achieved by insertion sort technique and a selection switch. The insertion sort technique provides only a capacitor index number (0 to N-1) in ascending order or descending order by measuring the SM capacitor voltages. Based on arm current direction, selection switch allows capacitor index number CI_{1-N} (ascending or descending order). This approach of generating capacitor index number is easy and extended to any SM level by simply changing the value of N (number of SMs) in insertion sorting c-script.

2) Generation of gate pulse pattern: The modulation signal generated from generalized space-vector block are compared with triangular carrier signals (PS-PWM or PD-PWM) and each output is added together to generate $N_{on} \ \epsilon \{1, 2...N\}$ which equal to the number of SMs to be turned on. The switching states for each SM for the upper arm (G_U) is generated by comparing the CI_{1-N} and N_{on}. Similarly, the switching states (G_L) for each SM for lower arm is generated by comparing the CI_{1-N} and $N - N_{on}$ satisfying Eq. (11). To maintain constant switching frequency, reduced switching frequency (RSF) approach presented in [23] is incorporated with this approach.

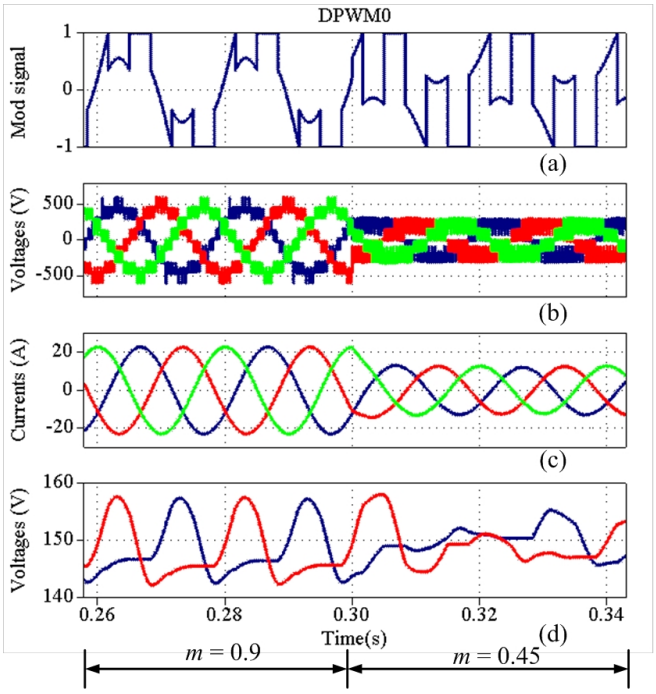

Fig. 6. Dynamic performance of DPWM0 at 50 Hz (a) Modulation signal (b) Output line-line voltages (c) Output currents (d) Upper and lower arm capacitor voltages.

IV. Simulation Results and Discussion

To validate the performance and the effectiveness of the proposed generalized SVPWM technique with SM capacitor voltage balancing algorithm, simulation studies have been carried out for 5-level three-phase MMC with HB-SMs (Fig. 3(a)) using PLECS software. The efficacy of proposed voltage balancing approach with PS-PWM scheme is simulated with passive load (R_L = 10 Ω, L_L = 20 mH) at an effective switching frequency f_s = 2 kHz and dc-link voltage V_{dc} = 600 V. Each arm have (N = 4) HB-SMs and each SM has one floating capacitor (C = 3.3 mF) with nominal voltages (V_c = 150 V). The dynamic performance of the proposed voltage balancing algorithm is demonstrated based on step change in modulation index (m) from 0.9 to 0.45 at t = 0.3 s with fundamental frequency f_1 = 50 Hz. The simulation results of all DPWM techniques (DPWM0, DPWM1, DPWM2, DPWM3) and SVPWM with their modulation signals are shown in Figs. 6-10. The

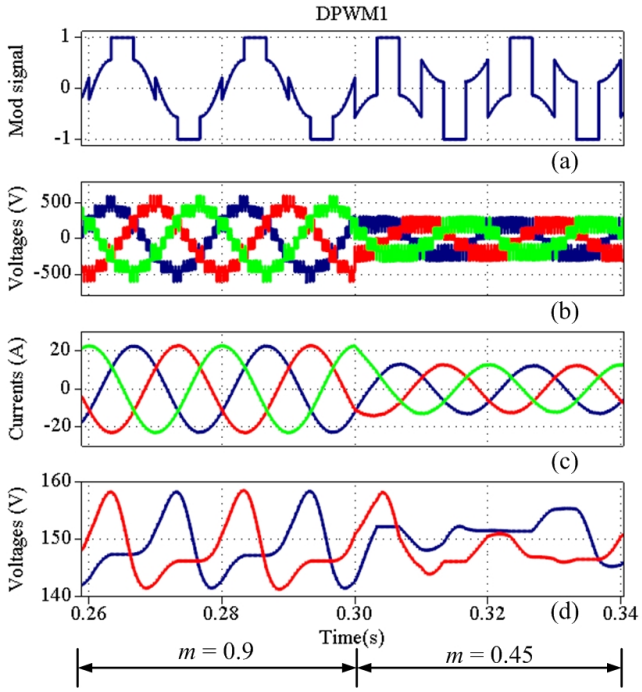

Fig. 7. Dynamic performance of DPWM1 at 50 Hz (a) Modulation signal (b) Output line-line voltages (c) Output currents (d) Upper and lower arm capacitor voltages.

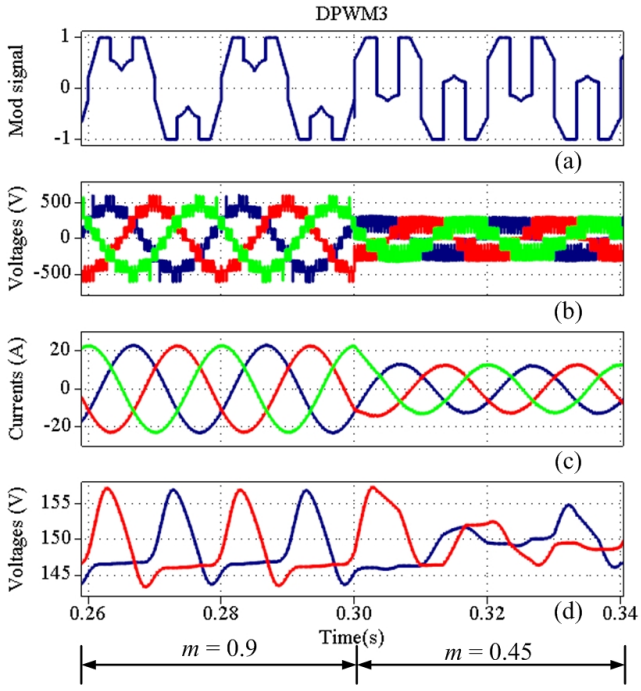

Fig. 9. Dynamic performance of DPWM3 at 50 Hz (a) Modulation signal (b) Output line-line voltages (c) Output currents (d) Upper and lower arm capacitor voltages.

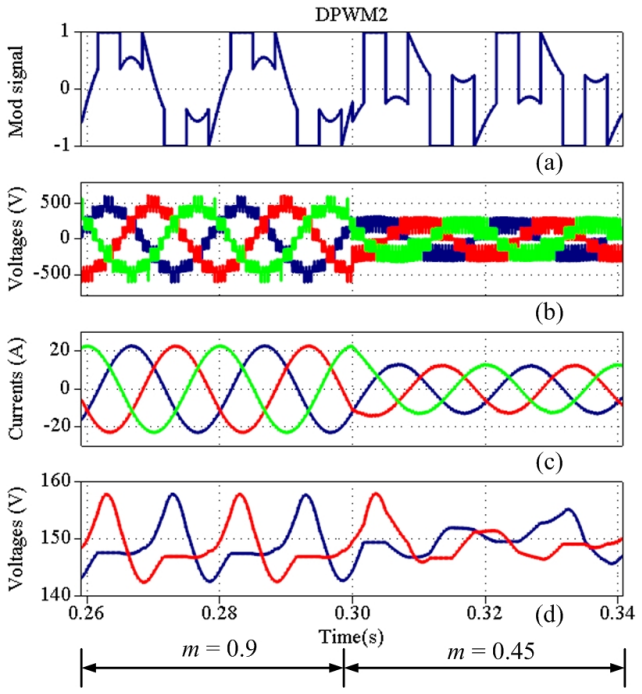

Fig. 8. Dynamic performance of DPWM2 at 50 Hz (a) Modulation signal (b) Output line-line voltages (c) Output currents (d) Upper and lower arm capacitor voltages.

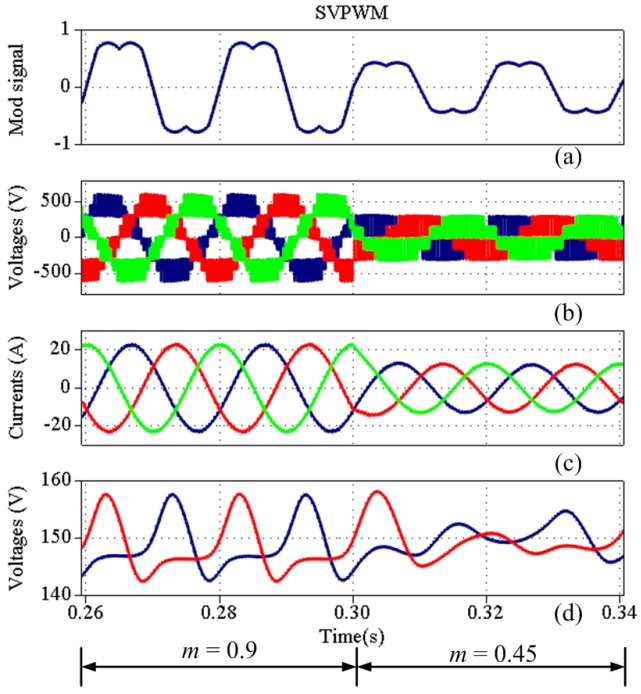

Fig. 10. Dynamic performance of SVPWM at 50 Hz (a) Modulation signal (b) Output line-line voltages (c) Output currents (d) Upper and lower arm capacitor voltages.

key performance of different DPWM techniques in terms of capacitor voltage ripple, waveform quality and dc-bus current compared with conventional SVPWM are depicted in Table II. The voltage ripple across the SM capacitors results in a negative sequence component current flows through the arms [22]. Compared to other techniques, the DPWM3 technique exhibits low capacitor voltage ripple thus lesser circulating currents. The circulating currents can be minimized by using

TABLE II
COMPARISON OF DIFFERENT DISCONTINUOUS PWM TECHNIQUES

Performance Index	SVPWM	DPWM0	DPWM1	DPWM2	DPWM3
Voltage THD (%)	27.4	19.8	20.6	19.5	18.9
DC-bus current ripple (RMS) [A]	16.08	16.10	16.14	16.08	16.06
Output current [A]	25.19	25.25	25.23	25.20	25.22
Capacitor voltage ripple (%)	12.92	14.76	13.12	13.10	11.63
Capacitor voltage ripple THD (%)	0.83	0.75	0.79	0.91	0.83

TABLE III
DC-BUS CURRENT RIPPLE ANALYSIS

PWM technique	DC (f_o)	$2f_1$	$4f_1$	$6f_1$	THD
SVPWM	16.07	0.537	0.022	0.589	8.210
DPWM0	16.10	0.015	0.003	0.009	7.229
DPWM1	16.13	0.779	0.007	0.236	4.881
DPWM2	16.07	0.387	0.185	0.823	4.270
DPWM3	16.03	0.218	0.108	1.361	22.21

active circulating current suppression controllers that use PI controllers in synchronous dq frame [23] or proportional-resonant (PR) controllers stationary $\alpha\beta$ frame [14] or model predictive methods [16]. Moreover, DPWM3 generates better waveform quality than other PWM techniques. In this paper, the dc-current ripple is chosen as the major criteria to evaluate performance of PWM technique as it is directly related to SM capacitor ripple and power losses. The dc-bus current ripple for all DPWM techniques is numerically analyzed and compared with SVPWM are listed in Table III. This analysis reveals that the DPWM3 technique exhibits higher efficiency as well as lower SM capacitor voltage ripple as it draws lesser dc-current from the source as depicted in Table III and Fig. 9. It is concluded that DPWM3 exhibits improved performance under steady-state and dynamic conditions compared to other DPWM techniques and is best suited for MMCs.

V. CONCLUSIONS

This paper presents a generalized SVPWM-based SM capacitor voltage balancing strategy for MMC and validation through simulation results. The results for DPWM techniques show effective balancing of the SM capacitor voltages at their reference values under dynamic conditions. This scheme can be easily extended to any SM type and any general n-level MMC. Moreover, it can be implemented with any PWM carriers (PS-PWM or PD-PWM). The performance of different DPWM techniques are compared with SVPWM and reveals that the DPWM3 technique exhibits improved performance among all DPWM techniques in terms of lower dc-current ripple, lower voltage THD and capacitor voltage ripple.

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