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A Pulsed Power Supply Adopting Active Capacitor Converter for Low-Voltage and Low-Frequency Pulsed Load

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***Abstract*—In a dc pulsed power supply (PPS), its instantaneous output power is pulsed, and its input power is required to be constant. In order to balance the instantaneous power difference, a storage capacitor is usually connected to the output terminal of the PPS. However, the storage capacitor is extremely large when the pulse repetition frequency is relatively low. In this paper, an active capacitor converter (ACC) is adopted in place of the storage capacitor. In the ACC, the storage capacitor is greatly reduced by intentionally increasing its voltage ripple. To improve the tracking ability of the terminal current of the ACC, a current reference feed-forward control scheme is proposed, and it is further simplified for avoiding the use of the reciprocal and square root circuits. In order to improve the dynamic response of the PPS when the pulsed load is triggered on and terminated, several methods are proposed. The methods of imposing a negative dc bias on the current reference and peak voltage control for the ACC storage capacitor are aiming for reducing the undershoot and overshoot of the output voltage, and two fast voltage loops are incorporated for limiting the maximum and minimum voltage of the storage capacitor in the ACC. Finally, a prototype with the output peak power of 2 kW, the output average power of 300 W, and the pulse repetition frequency of 150 Hz ~ 300 Hz is fabricated and tested to verify the validity of proposed PPS and control schemes.**

***Index Terms* —Pulsed power supply, active capacitor converter, tracking ability, current reference feed-forward scheme, peak voltage control.**

I. Introduction

Pulsed power supply (PPS) is one kind of special power supplies, which outputs periodical voltage or current with rectangular wave, triangular wave or trapezoidal wave, and it has been widely used in electrostatic precipitation [1], electroplating [2], pulse electrochemical wastewater treatment [3], [4] and radar transmitter [5]–[7]. According to the pulse repetition frequency (PRF), the PPS can be categorized into two types: high-frequency PPS and low-frequency PPS. The PPS can also be classified into high-voltage PPS and low-voltage PPS according to its output voltage level. In this paper, a high-power, low-frequency, low-voltage, and rectangular-wave PPS is studied, which outputs pulsed current with constant voltage.

As an interface between the power source and the pulsed load, the PPS should meet the following requirements: 1) The input current of the PPS is constant so that the low-frequency pulsed current does not propagate to the power source, which is especially important for photovoltaic panels to achieve high energy conversion efficiency and for fuel cells to extend its lifespan [8]–[10]; 2) When the pulsed load is being powered, the output voltage drop during the pulse cycle is small enough to ensure proper operation of the pulsed load [6], [7]; and 3) The PPS has high power density, which is very important, especially for the volume-critical and weight-critical applications. With constant output voltage and pulsed output current, the instantaneous output power of the PPS is pulsed. Meanwhile, the input current is required to be constant, thus the input power of the PPS is expected to be flat. To balance the instantaneous power difference, a storage capacitor is usually connected at the output terminal of the PPS. However, if the PRF is low, very large storage capacitors are required to achieve a small output voltage drop during the pulse cycle, leading to large size and heavy weight, and thus a low power density.

A bidirectional converter could be employed in place of the large storage capacitor for balancing the instantaneous input and output power difference, and it has been widely used in single-phase dc-ac inverters [11]–[14] and single-phase power factor correction (PFC) rectifiers [14]–[21]. By intentionally increasing the voltage ripple of the storage capacitor in the bidirectional converter, the storage capacitor could be significantly reduced. In voltage regulator (VR), a bidirectional converter is used to mitigate the voltage swing during the transients [22]–[24]. In addition, a bidirectional converter named adaptive active capacitor converter (AACC) is introduced for emulating a variable capacitor to stabilize the cascaded dc-dc converter system [25]. And the concept of the emulated variable capacitor is also presented in [26] and [27] to replace inflexible passive capacitors. Basically, the bidirectional converters mentioned above is to replace the undesired bulky capacitor and create an extra path for the unbalanced power. This approach can be also applied to the PPS, and the bidirectional converter is named active capacitor converter (ACC), which has been presented in [28]. This paper will provide more detailed design considerations for the PPS adopting the ACC.

The primary control objective of the ACC is to regulate its terminal current to provide the pulsed current except the dc component. A dual-loop control method is proposed in [20] for the ACC in LED driver (single-phase PFC rectifier) where the output current of the PFC converter is sinusoidal with twice the line frequency. In this method, a current loop is introduced to control the terminal current of the ACC and make it equal to the ac component of the output current of the PFC converter, and a voltage loop is used to regulate the voltage of the ACC storage capacitor. To improve the ACC terminal current tracking ability, a feed-forward control scheme is proposed in [21], in which the instantaneous expression of the duty cycle is calculated. Unfortunately, to

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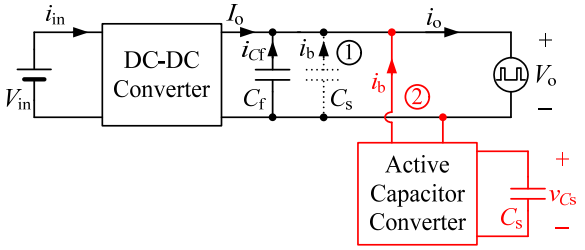

Fig. 1. Circuit configuration of the PPS with different locations of the storage capacitor.

realize the feed-forward function, an analog multiplier must be included to implement the reciprocal circuit and square root circuit, which makes the control circuit quite complicated.

For the PPS studied in this paper, the load current is rectangular, and it contains abundant harmonics at PRF and its multiples. In order to improve the tracking ability of the ACC terminal current, the feed-forward control scheme proposed in [21] is modified for the applications with an arbitrary load current in this paper. Furthermore, the expression of the duty cycle is linearized by applying the Taylor's approximation. In doing so, the multiplier can be removed and the control circuits can be simplified.

This paper is organized as follows. In Section II, the circuit configuration of the PPS is presented. The feed-forward control scheme for the ACC with an arbitrary load current is derived and simplified in Section III. The dynamic response of the PPS is analyzed and the methods for improving the dynamic response are given in Section IV. In Section V, the design of the ACC inductor and the output filter capacitor of the dc-dc converter are discussed. In Section VI, the experimental results from a prototype with output peak power of 2 kW, output average power of 300 W, and PRF of 150 Hz ~ 300 Hz are provided to verify the proposed control scheme. Finally, Section VII concludes this paper.

II. Circuit Configuration of the PPS

Fig. 1 shows the circuit configuration of the PPS, where the dc-dc converter converts the input dc voltage V_{in} to the desired dc output voltage V_o. The bandwidth of the dc-dc converter is generally designed to be quite low for the purpose of preventing the low-frequency pulsed output current from propagating to the input voltage source [29], [30]. In order to handle the pulsed power, a large storage capacitor, C_s, is directly connected in parallel with the output terminal of the PPS. The large storage capacitor can also be replaced by an ACC. Certainly, a storage capacitor is still required in the ACC. Noted that C_f is the output filter capacitor of the dc-dc converter to filter the switching-frequency current.

Fig. 2 shows the key operational waveforms of the PPS. The pulsed output current i_o is a rectangular waveform, where, I_p is the magnitude, T_p is the pulse repetition period, D_p is the pulse duty cycle, and I_o is the average output current. Since the output voltage V_o is constant, the instantaneous output power is pulsed. As mentioned above, the input current of the PPS, i_{in}, is expected to be controlled to be flat, so the input power of the PPS, P_{in}, is constant. i_b is the current provided by the storage capacitor.

No matter the storage capacitor is located at the output terminal or within the ACC, when $P_{in} > p_o$, the superfluous energy will charge the storage capacitor, and the storage capacitor voltage v_{Cs} increases; while when $P_{in} < p_o$, the

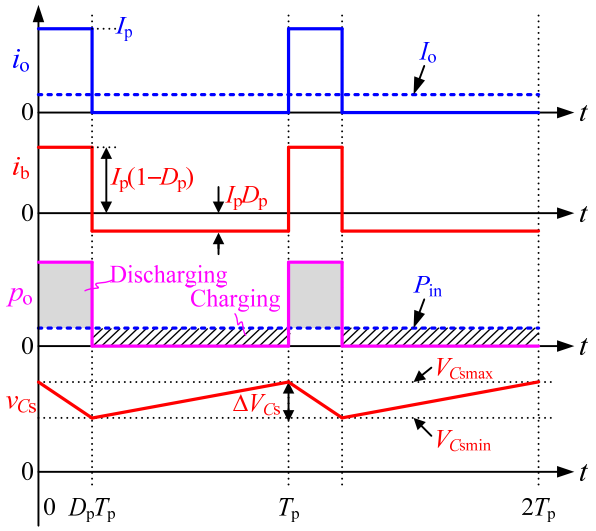

Fig. 2. Key operational waveforms of the PPS.

storage capacitor is discharged to provide the deficit, and v_{Cs} decays.

According to Fig. 2, the energy absorbed by the storage capacitor during one pulse cycle is

$$\Delta E_{Cs} = V_o D_p I_p \left(1 - D_p\right) T_p \tag{1}$$

ΔE_{Cs} can be also expressed as

$$\Delta E_{Cs} = \frac{1}{2} C_s V_{Cs\max}^2 - \frac{1}{2} C_s V_{Cs\min}^2 \tag{2}$$

where V_{Csmax} and V_{Csmin} are maximum and minimum voltages of the storage capacitor, respectively.

From (1) and (2), the capacitance of the storage capacitor can be derived as

$$\begin{aligned} C_s &= \frac{2V_o I_p D_p \left(1 - D_p\right)}{f_p \left(V_{Cs\max}^2 - V_{Cs\min}^2\right)} \\ &= \frac{V_o I_p D_p \left(1 - D_p\right)}{f_p \left(V_{Cs\max} - V_{Cs\min}\right)\left(V_{Cs\max} + V_{Cs\min}\right)/2} \\ &= \frac{V_o I_p D_p \left(1 - D_p\right)}{f_p \cdot \Delta V_{Cs} \cdot V_{Cs\_ave}} \end{aligned} \tag{3}$$

where, $f_p = 1/T_p$ is the PRF, $\Delta V_{Cs} = V_{Csmax} - V_{Csmin}$ is the voltage ripple across C_s, $V_{Cs\_ave} \approx (V_{Csmax} + V_{Csmin})/2$ is the average voltage of C_s. As seen from (3), the capacitance of the storage capacitor can be significantly reduced by intentionally increasing V_{Cs_ave} and/or ΔV_{Cs}.

Here, we take the PPS with 2 kW peak output power as an example to illustrate the design of the capacitance of the storage capacitor. Table I gives the key specifications of the PPS. When the storage capacitor is connected at the output terminal of the PPS, by substituting $V_{cs\_ave} = V_o = 28$ V, $\Delta V_{Cs} = 28$ V × 3%, $f_p = 150$ Hz, $D_p = 15\%$, $I_p = 71$ A into (3), it can be calculated that the required storage capacitor $C_s = 71.85$ mF.

When the ACC is adopted, a large voltage ripple on C_s is allowed since it is not restricted by the voltage drop during the pulse cycle. Letting $V_{Cs\_ave} = 48$ V, $\Delta V_{Cs} = 24$ V and substituting them together with $f_p = 150$ Hz, $D_p = 15\%$, $V_o = 28$V, $I_p = 71$A into (3), the required capacitance of the ACC storage capacitor is 1.47 mF, which is only 2.04% of the storage capacitance connected at the output terminal. Apparently, the storage capacitance could be significantly reduced when the ACC is adopted.

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TABLE I
KEY SPECIFICATIONS OF THE PPS

Parameters	Value
Input voltage V_{in} / V	100
Output Voltage V_o / V	28
Output peak current I_p / A	71
Pulse repetition frequency f_p / Hz	150 ~ 300
Pulse duty cycle D_p	≤ 15%
Allowed maximum output voltage drop ΔV_o	3%
Allowed minimum input current ΔI_{in} / A	0.5

III. PROPOSED CURRENT REFERENCE FEED-FORWARD CONTROL SCHEME FOR THE ACC

The dc-dc converter and the ACC are independently controlled. The control objective of the dc-dc converter is to restrain the low-frequency ripple in the input current of the dc-dc converter while regulating the output voltage. Various control strategies for the dc-dc converter have been discussed and compared in [29] and [30]. In this paper, a dual-loop control, which consists of an outer voltage loop and an inner filter inductor current loop, is employed for the dc-dc converter. By reducing the bandwidth of the outer voltage loop, the low-frequency ripple in the input current of the dc-dc converter can be reduced effectively. The design of the dual-loop control has been extensively discussed in previous publications, and it will not be repeated here.

A. Current Reference Feed-Forward Control Scheme for the ACC

Fig. 3 gives the topology and control schematic diagram of the ACC. Here, the ACC is a boost converter from the view of the output terminal of the PPS. A voltage and current dual-loop control method is used for the ACC with switch S_1 being opened and S_2 being turned to terminal 2, which is proposed in [20]. The current loop aims for controlling the terminal current of the ACC to make it equals to the ac component of the load current, and the voltage loop is used to regulate the storage capacitor voltage of the ACC. The output of the voltage regulator is added to the current reference to compensate the circuit losses. In order to eliminate the influence of the output of the voltage regulator on the current reference, the bandwidth of the voltage loop should be designed to be far lower than the PRF, and the output of the voltage regulator is approximately a dc value.

Referring to Fig. 2, the rectangular-wave load current contains abundant harmonics at the PRF and its multiples. Hence, to ensure an excellent current tracking ability, the gain of the current loop at the PRF and its multiples should be designed as high as possible, i.e., the bandwidth of the current loop should be designed high enough. However, for ensuring the system stability, the current loop bandwidth cannot be too high, making it difficult to achieve satisfactory current tracking ability. A feed-forward control scheme is proposed in [21] to improve the current tracking ability, yet it is only applicable to cases where the load current is sinusoidal. In this paper, the feed-forward control scheme is modified for to the cases with an arbitrary load current, which will be presented as follows.

According to Fig. 2, the energy that discharges C_s is

$$\Delta E_{Cs} = \int_0^t V_o i_b(t)dt \tag{4}$$

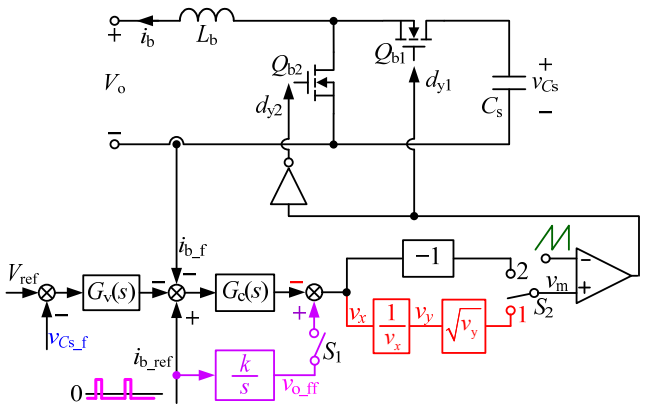

Fig. 3. Control schematic diagram of the ACC.

And ΔE_{Cs} can be also expressed as

$$\Delta E_{Cs} = \frac{1}{2}C_s V_{Cs\max}^2 - \frac{1}{2}C_s v_{Cs}^2(t) \tag{5}$$

Combining (4) and (5), the instantaneous voltage of C_s can be derived as

$$v_{Cs}(t) = \sqrt{-\frac{2}{C_s}\int_0^t V_o i_b(t)dt + V_{Cs\max}^2} \tag{6}$$

According to (6), the desired instantaneous duty cycle of switch Q_{b1} can be calculated as

$$d_{y1}(t) = \frac{V_o}{v_{Cs}(t)} = \frac{V_o}{\sqrt{-\frac{2}{C_s}\int_0^t V_o i_b(t)dt + V_{Cs\max}^2}} \tag{7}$$

The duty cycle of Q_{b1} is obtained by comparing the modulation signal with the sawtooth carrier signal. So, the needed modulation signal $v_m(t)$ is

$$\begin{aligned} v_m(t) &= d_{y1}(t)V_M = \frac{V_o V_M}{\sqrt{-\frac{2}{C_s}\int_0^t V_o i_b(t)dt + V_{Cs\max}^2}} \\ &= \frac{1}{\sqrt{k_1\int_0^t i_b(t)dt + k_2}} \end{aligned} \tag{8}$$

where, V_M is the amplitude of the saw-tooth carrier, and k_1 and k_2 are

$$k_1 = -\frac{2}{C_s V_o V_M^2} \tag{9}$$

$$k_2 = \frac{V_{Cs\max}^2}{V_o^2 V_M^2} \tag{10}$$

The terms k_1 and k_2 are constant when the parameters of the main circuits of the ACC are determined.

In order to produce the modulation signal according to (8) – (10) and incorporate it in the dual-loop control circuit, a feed-forward path and a calculation circuit, which consists of an integrator k/s, a reciprocal circuit and a square root circuit, is added, and then S_1 is closed and S_2 is turned to terminal 1, as shown in Fig. 3, where the term k is designed be equal to k_1. This is called the current reference feed-forward control scheme. It should be pointed out that the load current $i_b(t)$ in (8) can be arbitrary while the feed-forward control scheme proposed in [21] is only for the load current with sinusoidal waveform. For realizing the reciprocal circuit and square root circuit, analog multiplier is required, which makes the control circuit more complicated.

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B. Simplified Current Reference Feed-Forward Control Scheme for the ACC

Define

$$x = -\frac{2}{C_s}\int_0^t V_o i_b(t)dt + V_{Cs\max}^2 \tag{11}$$

Then, (8) can be rewritten as

$$v_m(x) = \frac{V_o V_M}{\sqrt{x}} \tag{12}$$

By applying Taylor's expansion on $1/\sqrt{x}$, $1/\sqrt{x}$ can be approximated as

$$\frac{1}{\sqrt{x}} = -\frac{1}{2\sqrt{x_0^3}}x + \frac{3}{2\sqrt{x_0}} \tag{13}$$

where $x_0 = \left(V_{Cs\min}^2 + V_{Cs\max}^2\right)/2$. The detailed derivation procedure is given in the Appendix.

According to (11) to (13), $v_m(t)$ can be approximated as

$$\begin{aligned} v_{m\_fit}(t) &= V_o V_M\left[\frac{3}{2\sqrt{x_0}} - \frac{1}{2\sqrt{x_0^3}}\left(-\frac{2}{C_s}\int_0^t V_o i_b(t)dt + V_{Cs\max}^2\right)\right] \\ &= V_o V_M\left[\frac{1}{C_s\sqrt{x_0^3}}\int_0^t V_o i_b(t)dt + \frac{3}{2\sqrt{x_0}} - \frac{1}{2\sqrt{x_0^3}}V_{Cs\max}^2\right] \\ &= k_1'\int_0^t i_b(t)dt + k_2' \end{aligned} \tag{14}$$

where

$$k_1' = \frac{V_o^2 V_M}{C_s\sqrt{x_0^3}} \tag{15}$$

$$k_2' = V_o V_M\left(\frac{3}{2\sqrt{x_0}} - \frac{1}{2\sqrt{x_0^3}}V_{Cs\max}^2\right) \tag{16}$$

The terms k_1' and k_2' are constant when the parameters of the main circuits of the ACC are determined. By letting V_o = 28 V, $V_{Cs\min}$ = 35 V, $V_{Cs\max}$ = 60 V, V_M = 1.8 V and substituting them together with C_s = 1.47 mF, D_p = 0.15, f_p = 150 Hz and f_p = 300 Hz into (8) and (14), respectively, the curves of $v_m(t)$ and $v_{m\_fit}(t)$ are depicted in Fig. 4. Note that "150" and "300" in the subscript denote the PRF. As seen, the fitting error is small and acceptable, so it is reasonable to replace $v_m(t)$ with $v_{m\_fit}(t)$.

In Fig. 3, when switch S_1 is closed and S_2 is turned to terminal 2, the control schematic diagram is for simplified current reference feed-forward control scheme, where, the term k is designed to be equal to $-k_1'$. The output of the current regulator can provide the term k_2' and the error between $v_m(t)$ with $v_{m\_fit}(t)$. Thus, the desired modulation signal shown as (8) can be obtained. As seen, the reciprocal circuit and square root circuit are no longer needed, leading to a simplified realization of the control circuit.

C. Control Circuits for Implementation of the Current Reference Feed-Forward Control Scheme

Based on previous analysis, Fig. 5 shows the detailed control circuit of the simplified current reference feed-forward control scheme, which are implemented by analog components.

In subcircuit A, the load current sampling signal i_{o_s} is first amplified by a differential amplifier comprising $R_1 - R_4$ and amplifier A_1. Then, the output of A_1 is sent to a one-order high-pass filter (HPF) composed of R_b, C_b and amplifier A_2 to extract the ac component of the pulsed load current, defined as i_{b_ref}, which is taken as a part of the current reference of i_b.

Subcircuit B is a peak value detection circuit, composed

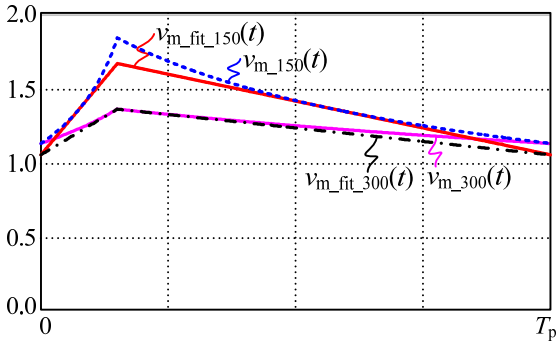

Fig. 4. Fitting curves of the modulation signals.

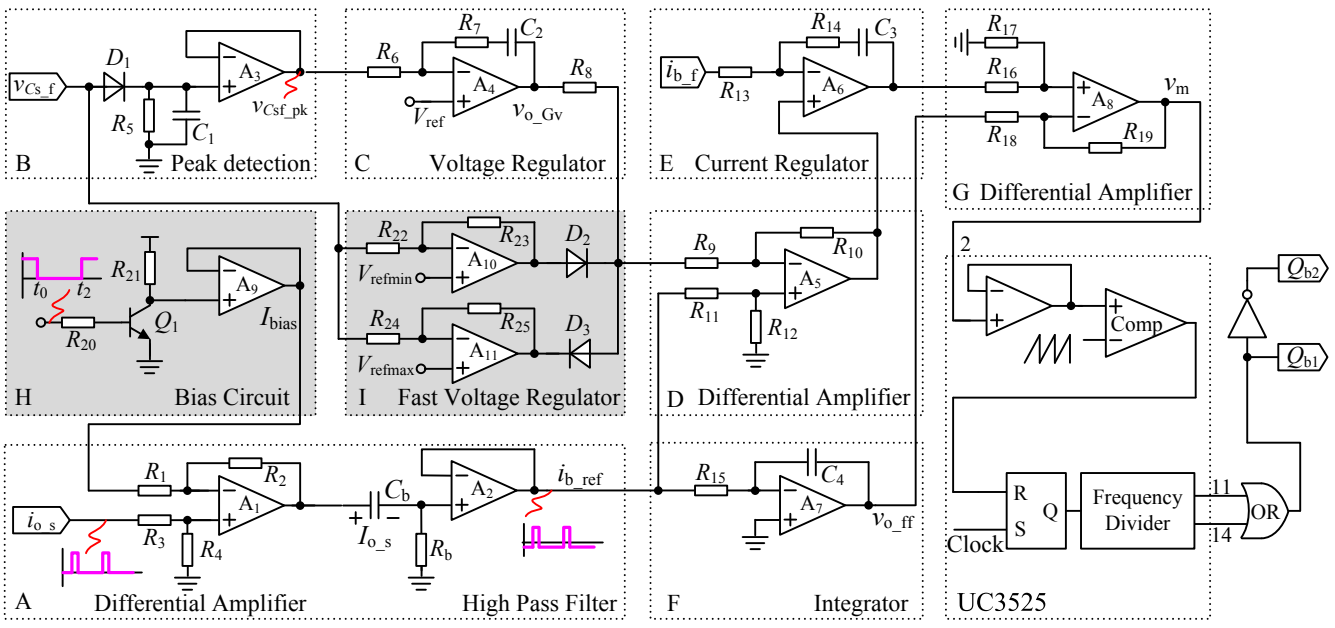

Fig. 5. Control circuit of the ACC.

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of D_1, R_5, C_1 and amplifier A_3, which detects the peak voltage of C_s. The purpose of detecting the peak voltage of C_s will be explained in Section IV. Subcircuit C is the voltage regulator. Here, a proportional-integral (PI) regulator is adopted, composed of R_6, R_7, C_2 and amplifier A_4. The output of the voltage regulator, v_{o_Gv}, is subtracted from i_{b_ref} with the differential amplifier (subcircuit D) and used as the actual current reference.

Subcircuit E is the current regulator, which is a PI regulator here, composed of R_{13}, R_{14}, C_3 and amplifier A_6, for forcing i_b to track the current reference. The output of the current regulator, v_{o_Gc}, will be used to provide the term k_2' in (14) and the error between $v_m(t)$ and $v_{m\_fit}(t)$. Subcircuit F is an integrator composed of R_{15}, C_4 and amplifier A_7. i_{b_ref} is sent to this integrator to obtain the first term in (14), defined as v_{o_ff}. Here, the product of R_{15} and C_4 is designed to be equal to $1/k_1'$. Subcircuit G is a differential amplifier, composed of $R_{16} - C_{19}$ and amplifier A_8, for realizing the reference current feed-forward control scheme and obtaining the modulation signal v_m. v_m is sent to the controller UC3525, and two drive signals are obtained. The two drive signals are then sent to the corresponding logic circuits, finally generating two complementary drive signals for switches Q_{b1} and Q_{b2}.

Subcircuits H and I in Fig. 5 are used for improving the dynamic performance of the PPS when the load is triggered on and terminated, which will be explained in Section IV.

IV. Solutions for Improving the Dynamic Response of the ACC

A. Dynamic Performance When the Pulsed Load is Triggered on and Terminated

As mentioned in Section III, the current reference of i_b is extracted from the pulsed load current via a noninverting amplifier and a one-order HPF. The transfer function of the one-order HPF is

$$G_{HPF}(s) = \frac{s}{s + 2\pi f_0} \tag{17}$$

where f_0 is the corner frequency of the HPF. The phase-shift introduced by the HPF is

$$\varphi = 90° - \arctan\frac{2\pi f}{2\pi f_0} = 90° - \arctan\frac{f}{f_0} \tag{18}$$

Therefore, the error between the output and input of the HPF is

$$I_{error} = \frac{I_{o\_s}\angle 0 - I_{o\_s}\angle\varphi}{I_{o\_s}\angle 0} = 2\sin\left(\frac{\varphi}{2}\right) \tag{19}$$

Combining (18) and (19), the corner frequency of the HPF should be designed less than 1% of the PRF if I_{error} is required to be smaller than 1% at the PRF. This leads to an extremely slow dynamic response of the HPF.

Fig. 6 shows the dynamic waveforms of the HPF, where, i_{o_s} and i_{b_ref} are the sensed pulsed load current and current reference for the ACC, respectively, i_{ref_ideal} is the desired current reference. As seen, when the pulsed load is triggered on at t_0, i_{b_ref} has a dc component during $[t_0, t_1]$ resulted by the HPF. Thus, the released energy from the ACC is larger than the absorbed energy in one pulse cycle. This will lead to the decrease of v_{Cs}, and v_{Cs} will decay to V_o. Then, the output filter capacitor C_f starts to release energy. Since C_f is

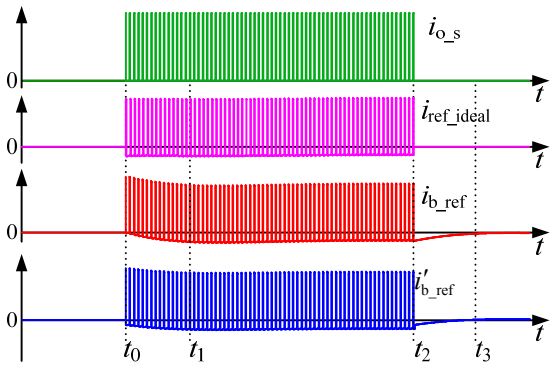

Fig. 6. Dynamic waveforms of high pass filter.

relatively small, there will be a large voltage undershoot.

When the pulsed load is terminated at t_2, the capacitor C_b in the HPF, as shown in subcircuit A in Fig. 5, is discharged through R_b during $[t_2, t_3]$, and i_{b_ref} is still negative. Thus, C_s will be charged and v_{Cs} increases. Due to the low bandwidth of the voltage loop, a large voltage overshoot will arise in v_{Cs}.

From the above analysis, it can be concluded that, when the pulsed load is triggered to work and is terminated, the dynamic response of PPS is poor due to the HPF and low bandwidth of the voltage loop. In order to improve the dynamic performance, several solutions are proposed as follows.

B. Solutions for Improving the Dynamic Performance

1) *Subtracting DC Bias from the Current Reference*

The function of the HPF is to remove the dc components I_{o_s} from i_{o_s}. If i_{o_s} is a pure ac component, shown as i'_{ref_ideal} in Fig. 6, the response time of the HPF would be zero. Hence, if a negative bias I_{bias} is imposed on i_{o_s} in advance, the response time of the HPF can be shortened effectively, shown as i'_{b_ref} in Fig. 6. Subcircuit H in Fig. 5 shows the implementation of this method. The transistor Q_1 is controlled by the pulsed load trigger signal. When the pulsed load is triggered to work at t_0, Q_1 is turned off and the negative bias I_{bias} is imposed. When the pulsed load is terminated at t_2, Q_1 is turned on and the bias I_{bias} is removed.

Nevertheless, the dc component I_{o_s} varies with the magnitude of the pulsed load. When the magnitude of the pulsed load is low, i.e., at light load, I_{o_s} is nearly zero. Under this load condition, if I_{bias} is chosen to be too large, the energy provided by the ACC is insufficient, and C_f will be discharged when the pulsed load is triggered on, leading to a large voltage undershoot. So, a tradeoff should be made between light load and heavy load conditions when choosing the value of I_{bias}. Here, I_{bias} is set to half of the maximum value of I_{o_s} at full load.

2) *Peak Voltage Control for the ACC Storage Capacitor Voltage*

The dc-dc converter is designed to provide the average power and has no capability of providing the pulsed power. To gain a good dynamic performance, the energy stored in the storage capacitor in the ACC when the pulsed load is at off state should be enough, so as to provide the deficit between the pulsed load and the output power of the dc-dc converter when the pulsed load is triggered on. So, it is better to regulate the peak voltage of the ACC storage capacitor at the desired value. To enforce this, the peak voltage control is used here, and a peak value detection

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circuit (subcircuit B), as shown in Fig. 5, is added to detect the peak voltage of v_{Cs}.

3) *Limiting of the Maximum and Minimum Voltage of C_s*

As aforementioned, the bandwidth of the ACC voltage loop is designed much lower than the PRF to mitigate its influence on the reference of the ACC terminal current. This will result in a large overshoot or undershoot in v_{Cs} when the load is triggered on and terminated, and even causes damage to the power devices in the ACC. To address this issue, two fast voltage loops, which usually adopt a proportional regulator, are introduced to limit the maximum voltage (slightly higher than the nominal value) and minimum voltage (slightly lower than the nominal value), respectively, as shown in Fig. 5 (subcircuit I). When the storage capacitor voltage exceeds the upper limit, the voltage loop used to limit the maximum value will be put into service. When the storage capacitor voltage reaches the lower limit, the voltage loop used to limit the minimum value will put into service. Obviously, the three voltage loops shown in Fig. 5 can transition smoothly among each other.

Likewise, two fast voltage loops can be also be introduced to limit the maximum and minimum voltage for the dc-dc converter.

V. Design of the Inductor in the ACC and the Filter Capacitor of the DC-DC Converter

The design of the dc-dc converter is similar to the regular dc-dc converter except for the output filter capacitor C_f, and it will not be discussed here. In the following, only the design of the inductor in the ACC and the output filter capacitor C_f are given.

A. Design of the Inductor in the ACC

In order to reduce the conduction loss of the power switches in the ACC, the current ripple of the inductor in the ACC is preferred to be small. However, too small current ripple means a large inductor, which will leads to a large size and deteriorate the dynamic response. Hence, a tradeoff should be made when designing the inductor. Here, the current ripple is chosen as 20% of the average value.

The inductor in the ACC can be calculated as [20]

$$L_b = \frac{(v_{Cs}(t) - V_o)V_o}{f_s \cdot \Delta i_{Lb} \cdot v_{Cs}(t)} \tag{20}$$

where, f_s is the switching frequency, Δi_{Lb} is the inductor current ripple. Here, the switching frequency is chosen as 100 kHz. Then, according to (6) and (20), the curve of the inductance in the ACC in one pulse cycle is depicted, as shown in Fig. 7. Hence, we choose the inductor as 12.6μH.

B. Design of the Output Filter Capacitor

The inductor in the ACC limits the increasing slope of the terminal current of the ACC, i_b, as shown in Fig. 8. Thus, at the rising edge of the pulsed load current, the output filter capacitor of the PPS, C_f, is discharged to provide the deficit, causing its voltage to decrease. At the falling edge of the pulsed load current, C_f is charged to absorb the surplus current, causing its voltage to increase. Note that the voltage drop of C_f at the rising edge is the voltage drop during the pulse cycle. So, the output filter capacitor C_f should be properly designed to ensure the voltage drop meets the requirements within the pulse cycle.

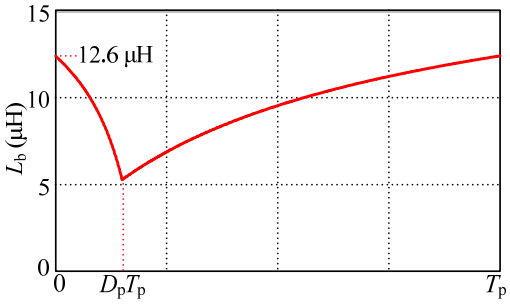

Fig. 7. Curve of the inductance in the ACC.

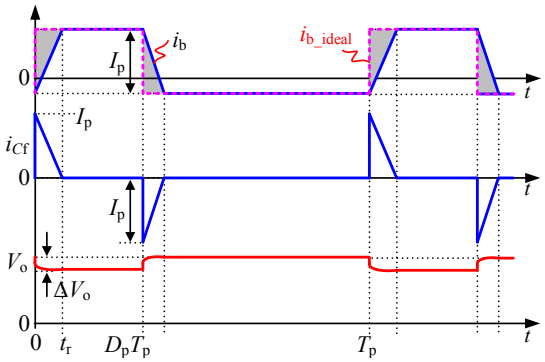

Fig. 8. Waveforms of the ACC terminal current tracking the current reference.

As seen in Fig. 8, at the rising edge of the pulsed load current, the top switch of the ACC, Q_{b1}, starts to conduct. Thus, the ACC terminal current i_b increases linearly and it increases to the desired value $I_p(1–D_p)$ at t_r. t_r can be expressed as

$$t_r = \frac{L_b \cdot \Delta I_{Lb}}{V_{Cs\max} - V_o} = \frac{L_b I_p}{V_{Cs\max} - V_o} \tag{21}$$

Letting V_{Csmax} = 60 V and substituting it together with L_b = 12.6 μH, V_o = 28 V, I_p = 71 A into (21), we have t_r = 27.96 μs.

During [0, t_r], C_f will be discharged to provide deficit, and the current of C_f is expressed as

$$i_{Cf}(t) = I_p - \frac{I_p}{t_r}t \tag{22}$$

The voltage drop of C_f is

$$\Delta V_o(t) = i_{Cf}R_{esr} + \frac{1}{C_f}\int_0^t i_{Cf}dt \tag{23}$$

where, R_{esr} is the ESR of the output filter capacitor C_f.

Substitution of (22) into (23), yields

$$\Delta V_o(t) = -\frac{I_p}{2C_f t_r}t^2 + \left(\frac{1}{C_f} - \frac{R_{esr}}{t_r}\right)I_p t + I_p R_{esr} \tag{24}$$

According to (24), the maximum output voltage drop during the pulse cycle is

$$\Delta V_o = \begin{cases} \dfrac{I_p}{2C_f t_r}(t_r - C_f R_{esr})^2 + I_p R_{esr} & t_r > R_{esr}C_f \\ I_p R_{esr} & t_r \le R_{esr}C_f \end{cases} \tag{25}$$

For an electrolytic capacitor, the product of R_{esr} and C_f equals to 60 μs [31], which is larger than t_r (= 27.96 μs). So, according to (25), the maximum output voltage drop during the pulse cycle is $\Delta V_o = I_p R_{esr}$. Considering ΔV_o = 28 V × 3%, I_p = 71 A, the maximum allowed ESR can be calculated as R_{esr} = 11.8 mΩ. Therefore, C_f = 5 mF is chosen.

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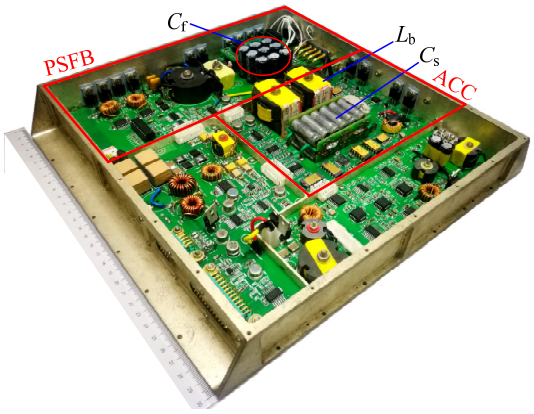

Fig. 9. Photograph of the prototype of the PPS.

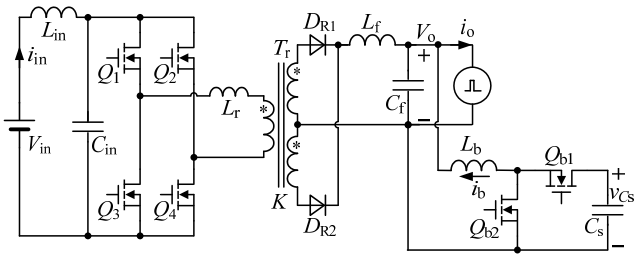

Fig. 10. Main circuit of the PPS.

VI. Experimental Verification

In order to verify the validity of the proposed PPS adopting the ACC and the control methods, a prototype, shown in Fig. 9, is fabricated and tested in the lab with the specifications listed in Table I. Fig. 10 shows the main circuits of the PPS, where the popular phase-shifted full-bridge (PSFB) converter is adopted as the dc-dc converter. In order to filter the switching-frequency current ripple, an input *LC*-filter composed of L_{in} and C_{in} is introduced. Both the PSFB converter and the ACC operate at the switching frequency of 100 kHz. The parameters of the PSFB converter are listed in Table II.

A. Volume and Cost Comparison Between the Proposed PPS and Conventional PPS

In conventional PPS with bulky storage capacitor connects at the output terminal of the PPS, 266 60-V/270-μF tantalum capacitors (135D277X0060K6) from Vishay are used for C_s. When the ACC is adopted, only 18 125-V/82-μF tantalum capacitors (135D826X0125K6) from Vishay are needed for C_s, and another 18 60-V/270-μF tantalum capacitors (135D277X0060K6) from Vishay are needed for C_f. The 60-V/270-μF and 125V-82μF tantalum capacitors have the same package. The inductor in the ACC is separated into two inductors connected in series here, and two sets of PTS40 ferrite cores from DMEGC are employed. Four MOSFETs (IPP110N20N3G) from Infineon are selected for the main switches of the ACC, and two MOSFETs are connected in parallel for each switch.

The volume and the cost comparison between two approaches, excluding the PSFB converter, are given in Table III. Note that all the prices for the devices and components are from Mouser Electronics Corporation. As seen, the volume and cost of the ACC are only 25.5% and 13.5% of the storage capacitance connected at the output terminal, respectively. So, the proposed PPS with the ACC has a reduced size and cost compared with the PPS with bulky storage capacitor.

TABLE II
PARAMETERS OF THE PHASE-SHIFTED FULL-BRIDGE CONVERTER

PSFB converter (100V – 28V, 300W, 100 kHz)			
Parameters	Value	Parameters	Value
$Q_1 \sim Q_4$	IPP600N25N3G	L_f	21 μH
$D_{R1} \sim D_{R2}$	MBR20200CT	C_f	5 mF
L_r	6.5 μH	L_{in}	40 μH
K (N_p/N_s)	8/3	C_{in}	40 μF

TABLE III
COMPARISON OF THE VOLUME AND COST BETWEEN THE ACC AND THE BULKY STORAGE CAPACITOR

Bulky storage capacitors for the PPS			
Parameters	Type	Volume	Cost
C_s	135D277X0060K6 (60V/270μF) × 266	1.93 mL × 266	$ 82.61 × 266
Total		0.51 L	$ 22000
ACC for the PPS			
Parameters	Type	Volume	Cost
$Q_{b1} \sim Q_{b2}$	IPP110N20N3G × 4	0.29 mL × 4	$ 4.63 × 4
C_f	135D277X0060K6 (60V/270μF) × 18	1.93 mL × 18	$ 82.61 × 18
C_s	135D826X0125K6 (125V/82μF) × 18	1.93 mL × 18	$ 82.61 × 18
L_b	DMEGC PTS40 × 2	31.42 mL × 2	$ 1.0 × 2
Total		0.13 L	$ 2990

B. Experiment Results

When the ACC adopts the dual-loop control method proposed in [20], the steady-state experimental waveforms with output peak power of 2 kW, pulse duty cycle of 15%, and PRF of 150 Hz and 300 Hz are shown in Fig. 11(a) and (b), respectively, where, v_o is the output voltage of the PPS, v_{Cs} is the voltage across C_s, i_{in} is the input current of the PPS, i_b is the current of L_b. As seen, the maximum output voltage drop during the pulse cycle is 1.1 V, and the maximum input current ripple is 0.1 A. Obviously, the PSFB converter only provides the average power, which is well in agreement with the theoretical analysis. Furthermore, the maximum value of v_{Cs} remains the same at different load conditions. Note that, only the waveforms at full load condition are given here since full-load condition is the worst case.

Fig. 12 shows the steady-state experimental waveforms with the original current reference feed-forward control scheme employed for the ACC. It can be seen that maximum output voltage drop during the pulse cycle is 0.52 V and the maximum input current ripple is 0.08 A. By comparing Figs. 11 and 12, it can be seen that the first dip on the output voltage V_o is nearly the same and it is independent of the PRF. This is because that the inductor in the ACC limits the increasing slope of the terminal current of the ACC, and C_f provides the deficit. However, as seen in Fig. 11, after the first dip, the output voltage is still decaying with the conventional dual-loop control scheme. And the decrease of the output voltage when the PRF is 150 Hz is larger than that when the PRF is 300 Hz. Comparatively, as seen in Fig. 12, after the first dip, the output voltage recovers when the proposed current reference feed-forward control scheme is adopted. This verifies that the proposed current reference feed-forward control scheme can improve the current tracking ability.

Fig. 13 shows the steady-state experimental waveforms

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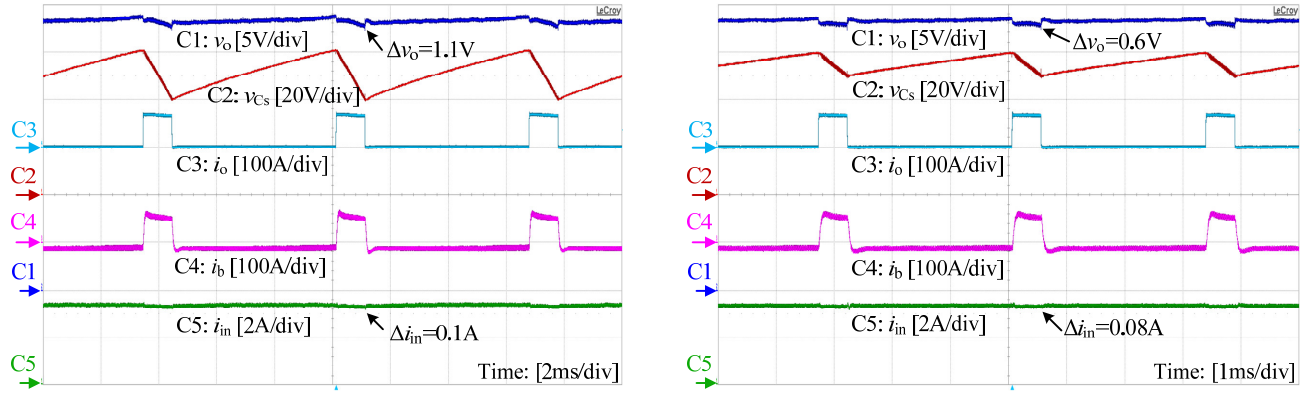
with the simplified current reference feed-forward control scheme for the ACC. As seen, the maximum output voltage drop during pulse cycle is 0.57 V and the maximum input current ripple is only 0.08 A, which is very close to the experimental waveforms shown in Fig. 12. This means the simplification of the feed-forward function does not deteriorate the current tracking ability.

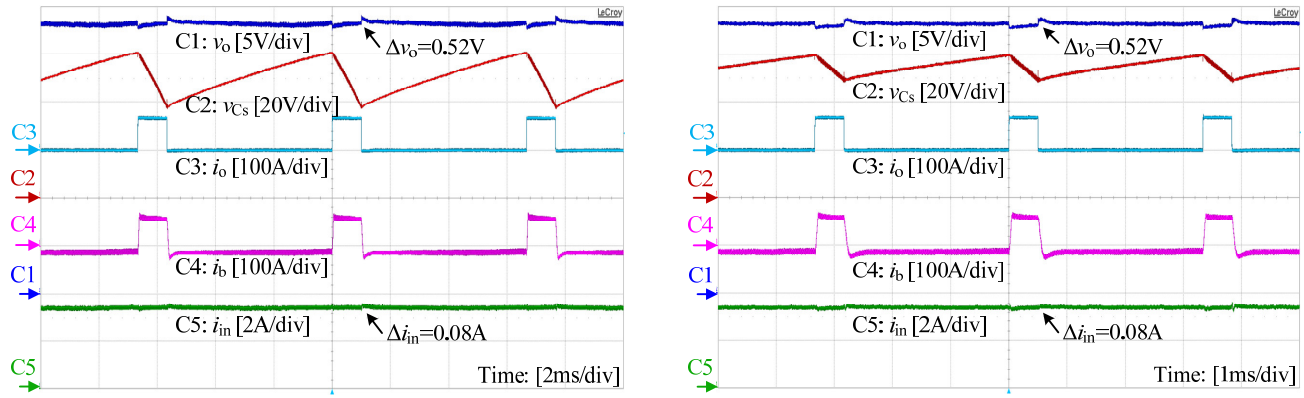
Fig. 14(a) shows the dynamic experimental waveforms when the pulsed load is triggered on and terminated, where, the duty cycle of the pulse is 15% and the PRF is 150 Hz. Here, the peak voltage control is used for the ACC. As seen, the voltage undershoot is 8.5 V when the pulsed load is triggered on and the voltage overshoot is 16.8 V when the pulsed load is terminated. Such a large undershoot and overshoot will weaken the performance of the pulsed load, and even damage the power devices in the PPS. Fig. 14(b) shows the dynamic experimental waveforms when the load is triggered on and terminated with the methods proposed in Section IV. As seen, both the voltage undershoot and overshoot are about 2.5 V when the pulsed load is triggered on and terminated, respectively, which are significantly reduced compared with that shown in Fig. 14(a). Thus, the dynamic response is greatly improved.

Fig. 15 shows measured conversion efficiency curves of the PPS. As seen, the efficiency of the PPS with the ACC is lower than that of the PPS with bulky storage capacitor. This is due to the additional power loss resulted by the ACC for handling the reactive power and processed reactive power is much higher than the average power of the PPS. However, with the use of ACC, the power density of the PPS is increased and cost is reduced. So, the decrease of the efficiency is acceptable.



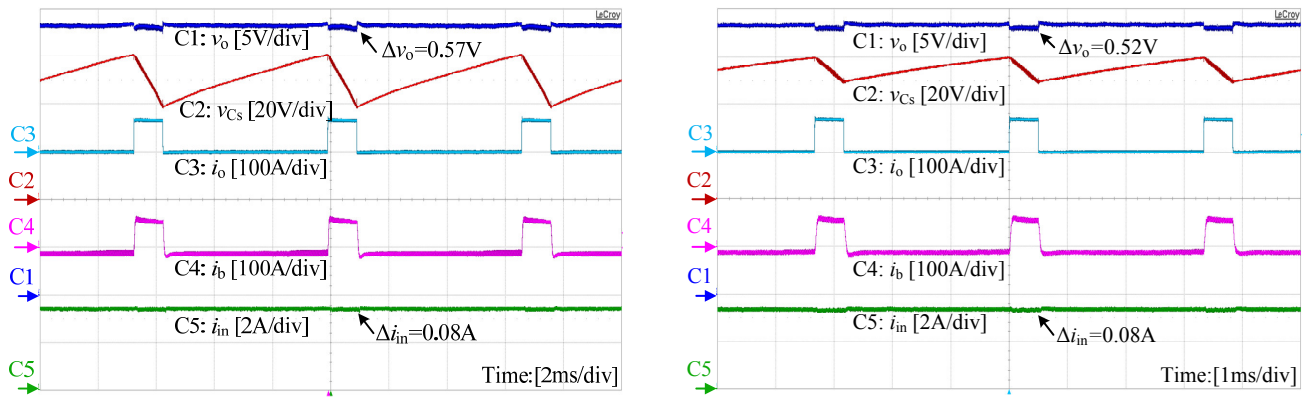
(a) (b)

Fig. 11. Steady-state experimental waveforms with dual-loop control scheme proposed in [20] for ACC. (a) 150 Hz-15%-full load. (b) 300 Hz-15%-full load.



(a) (b)

Fig. 12. Steady-state experimental waveforms with the original current reference feed-forward control scheme for ACC. (a) 150Hz-15%-full load. (b) 300Hz-15%-full load.



(a) (b)

Fig. 13. Steady-state experimental waveforms with the simplified current reference feed-forward control scheme for ACC. (a) 150Hz-15%-full load. (b) 300Hz-15%-full load.

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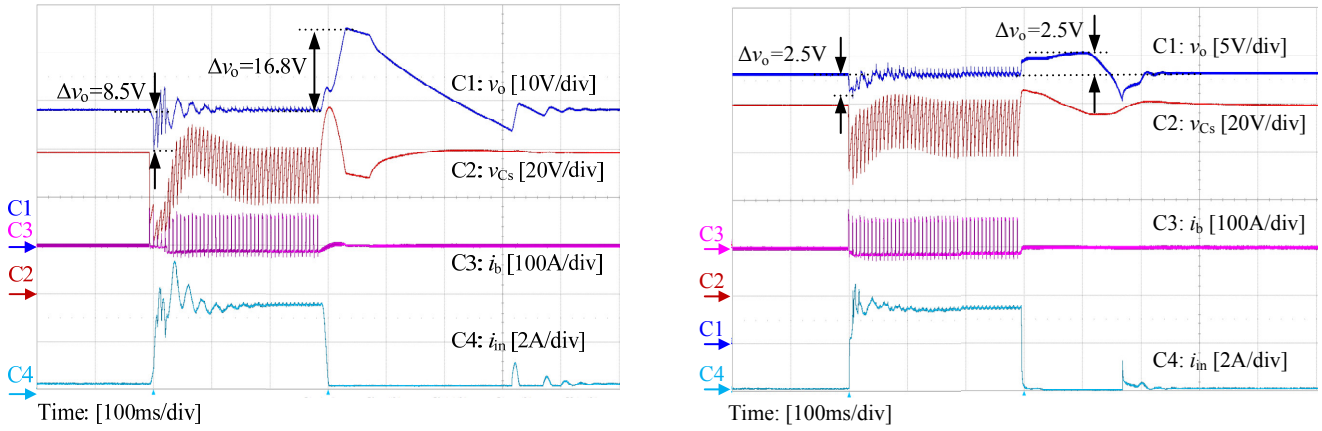

Fig. 14. Dynamic experimental waveforms. (a) Only with peak voltage control. (b) With the methods proposed in Section IV-B.

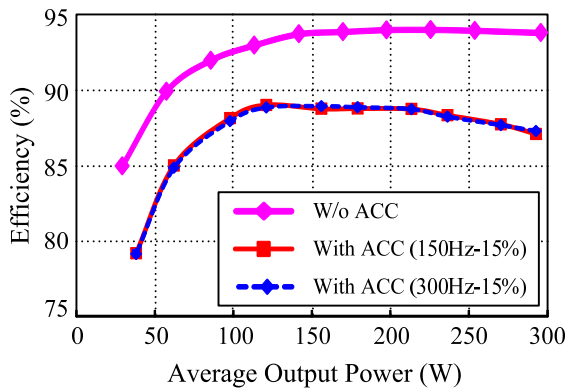

Fig. 15. Conversion efficiency of the PPS.

VII. Conclusion

In this paper, a boost-type ACC is adopted in place of the bulky storage capacitor for the pulsed power supply (PPS) to provide the pulsed power. By intentionally increasing its voltage ripple, the storage capacitor in the ACC can be significantly compared with the storage capacitance connected at the output terminal. Thus, the size of the PPS is greatly reduced and the power density is greatly increased. A current reference feed-forward control scheme, in which the instantaneous expression of the duty cycle is calculated, is proposed to achieve an excellent current tracking ability for the ACC, and it is further simplified for avoiding the use of multiplier, leading to a simple implementation of the control circuit. Furthermore, to improve the dynamic response of the PPS when the pulsed load is triggered on and terminated, three methods are proposed, including imposing a negative dc bias on the current reference, a peak voltage control for regulating the peak voltage of the ACC storage capacitor, and two fast voltage loops incorporated for limiting the maximum and minimum voltage of the storage capacitor in the ACC. Finally, the experimental results are provided to verify the validity of proposed PPS and control schemes.

Appendix

This Appendix provides the derivation process of the approximated expression of the function of $1/\sqrt{x}$, which is based on the Taylor's expansion method, and the choose of the expansion point of the Taylor's expansion is also given.

By applying Taylor's expansion on $1/\sqrt{x}$ at $x = x_0$, we have

$$\frac{1}{\sqrt{x}} = \frac{1}{\sqrt{x_0}} - \frac{1}{2x_0\sqrt{x_0}}(x-x_0) + \frac{3}{8x_0^2\sqrt{x_0}}(x-x_0)^2 + \cdots = \frac{1}{\sqrt{x_0}}\left[1 - \frac{1}{2x_0}(x-x_0) + \frac{3}{8x_0^2}(x-x_0)^2 + \cdots\right] \tag{A1}$$

Neglecting the high-order terms and keeping only the constant term and the first-order term, $1/\sqrt{x}$ is approximated as

$$\frac{1}{\sqrt{x}} \approx \frac{1}{\sqrt{x_0}} - \frac{1}{2\sqrt{x_0^3}}(x-x_0) = -\frac{1}{2\sqrt{x_0^3}}x + \frac{3}{2\sqrt{x_0}} \tag{A2}$$

The error resulted by the approximation is

$$e(x) = \frac{1}{\sqrt{x}} - \left(-\frac{1}{2\sqrt{x_0^3}}x + \frac{3}{2\sqrt{x_0}}\right) \tag{A3}$$

By differentiating $e(x)$, we have

$$e'(x) = \frac{1}{2\sqrt{x_0^3}} - \frac{1}{2\sqrt{x^3}} \tag{A4}$$

As seen in (A4), if $x > x_0$, $e'(x) > 0$; while if $x < x_0$, $e'(x) < 0$. Therefore, the minimum value of $e(x)$ occurs at $x = x_0$, and it is zero according to (A3). Thus, we can conclude that $e(x) \geq 0$.

According to (A3), integrating $e(x)$ in the range of the value of x, yields

$$e_{\text{int}}(x_0) = \int_{x_{\min}}^{x_{\max}} e(x)dx = 2\left(\sqrt{x_{\max}} - \sqrt{x_{\min}}\right) + \frac{1}{4\sqrt{x_0^3}}\left(x_{\max}^2 - x_{\min}^2\right) - \frac{3}{2\sqrt{x_0}}\left(x_{\max} - x_{\min}\right) \tag{A5}$$

where $x_{\min}$ and $x_{\max}$ are the minimum and maximum values of x, respectively. By differentiating $e_{\text{int}}(x_0)$, we have

$$e'_{\text{int}}(x_0) = \frac{3}{4\sqrt{x_0^5}}\left(x_{\max} - x_{\min}\right)\left(x_0 - \frac{x_{\max} + x_{\min}}{2}\right) \tag{A6}$$

As seen in (A6), if $x_0 > (x_{\max} + x_{\min})/2$, $e_{\text{int}}'(x_0) > 0$; while if $x_0 < (x_{\max} + x_{\min})/2$, $e_{\text{int}}'(x_0) < 0$. Therefore, the minimum value of $e_{\text{int}}(x_0)$ occurs when $x_0 = (x_{\max} + x_{\min})/2$. That is to say, the fitting accuracy of the approximated expression of $1/\sqrt{x}$, as given in (A2) is optimal when

$$x_0 = \left(x_{\min} + x_{\max}\right)/2 \tag{A7}$$

If x is defined as (11) in Section III-B, we have

$$x_{\min} = V_{\text{Csmin}}^2, \quad x_{\max} = V_{\text{Csmax}}^2 \tag{A8}$$

Thus, we have

$$x_0 = \left(V_{\text{Csmin}}^2 + V_{\text{Csmax}}^2\right)/2 \tag{A9}$$

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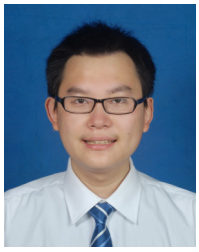

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