Low-Latency Image Acquisition and Processing with a Programmable Vision-System-on-Chip
ABSTRACT

This work aims to demonstrate the benefits of using a Vision-System-on-Chip for image processing tasks with very high latency demands between image acquisition and processing. By leveraging a column-parallel, mixed-signal data path, which is entirely software-defined by three application-specific instructionset processors (ASIPs), image data within multiple regions of interest can be analyzed at a frame rate of 5 kHz. Thus, with a delay of 0.44 ms, the trajectory of a moving object is analyzed and the object is precisely deflected using a solenoid.

Index Terms—image sensor, Vision-System-on-Chip, VSoC, ASIP, low latency, actuator control, trajectory prediction
EXISTING SYSTEM

• A novel Vision-System-on-Chip (VSoC) with column-parallel, mixed-signal data processing and a flexible digital interface.

• With three dedicated, stack-based application-specific instruction-set processors (ASIPs), this system allows for executing entirely software-defined, complex image processing algorithms at very high image rates.

• Due to the transfer function of the VSoC’s charge-based pixel cells exhibiting linear-logarithmic characteristics, its dynamic range is above 120 dB.
PROPOSED SYSTEM

• Conventional image processing systems consisting of an image sensor and a dedicated processing unit (PC and/or FPGA), this approach allows for implementing complex vision-based control tasks using solely the VSoC and its general-purpose interfaces, without having to rely on external hardware.

• In the final step, additional readout and/or exposure steps can be performed in high resolution and with high accuracy or in collaboration with the actuators (e. g. lock-in measurement with mechanical stimuli or switching wavelength range)
SYSTEM REQUIREMENTS

• HARDWARE REQUIREMENTS:
  • Processor - intel core i3
  • RAM - 2GB
  • Hard Disk - 20 GB

• SOFTWARE REQUIREMENTS:
  • Tool - MATLAB R2016
  • Operating system - Windows 7,8
REFERENCE


