

High-Quality UHD Demosaicing on Low-Cost FPGA

MICANS INFOTECH

ABSTRACT

In our time more and more digital camera developers are beginning to use UHD resolution. This way of design evolution allows us to greatly increase overall quality of captured image. With increasing of total pixel amount, we can implement new features without dramatic resolution loss, like digital zoom or geometric aberration correction. While resolution and quality grows, either does pipeline bandwidth of video processor. In 12G-SDI video stream, pixel clock is 596 MHz, which is defining while choosing FPGA, where our video processor will be implemented in. Intel and Xilinx recommends to use very high-cost FPGA, like: Arria, Stratix, Virtex and Kintex. In this paper, we will present an approach to design a pipeline that will process demosaicing of 4K 60 FPS video stream on low-cost FPGA Intel Cyclone V.

EXISTING SYSTEM

- In existing system, trivial method is bilinear interpolation.
- Regarding that in this method resolution is increased in every channel comparing to the nearest neighbor algorithm.
- Because of predicting values instead of copying them, the problem of aliasing arises, which leads to unwelcome color artifacts.

PROPOSED SYSTEM

- In our work, we will develop an approach to design an image processing pipeline using a combination of the algorithms named above for video with pixel clock rate up to 596 MHz.
- The base of this method is window forming module, which allows to parallelize data stream due to minimize operating clock frequency.
- Due to need of random one-time access to pixel values we can only use register memory for the window.

SYSTEM REQUIREMENTS

HARDWARE REQUIREMENTS:

- Processor - intel core i3
- RAM - 2GB
- Hard Disk - 20 GB

SOFTWARE REQUIREMENTS:

- Tool - MATLAB R2016
- Operating system - Windows 7,8

REFERENCE

- [1] B. E. Bayer, “Color Imaging Array,” U.S. Patent 3 971 065, 1976.
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