Coding For Improved Throughput Performance In Network Switches

ABSTRACT

- Network switches and routers need to serve packet writes and reads challenge the most advanced memory technologies

  scaling the switching rates parallelizing the packet I/Os using multiple memory units
- study of coded network switches, and in particular, how to design them to maximize the throughput advantages over standard uncoded switches
- contributes a variety of algorithmic and analytical tools to improve and evaluate the throughput performance
- placement of packets in the switch memory is the key to both high performance an algorithmic efficiency
- “design placement” is shown to enjoy the best combination of throughput performance and implementation feasibility

EXISTING SYSTEM

- Network switches and routers need to serve packet writes and reads at rates that challenge the most advanced memory technologies
- memory unit scaling the switching rates is commonly done by parallelizing the packet I/Os using multiples

DISADVANTAGE

unit scaling the switching rates is commonly done by parallelizing the packet I/Os using multiples

PROPOSED SYSTEM

- “design placement” is shown to enjoy the best combination of throughput performance and implementation feasibility
- variety of algorithmic and analytical tools to improve and evaluate the throughput performance

ADVANTAGES

- Design placements introduced
- Variety of algorithm and analytical tool to improve